

Quick Start for Advanced Design System (ADS) in Power Electronics Applications

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Keysight EEs of EDA

Evaluate ADS for design of power electronics

New devices (SiC, GaN) and their fast edges require new thinking about EDA tools

- Need Harmonic Balance: Yields steady state solution rapidly
- Three reasons to apply an EM field solver to your “virtual prototype”:
 1. PCB traces and vias add significant parasitic impedances to your circuit
 2. Create EM-based models of integrated magnetics
 3. Model EMI/EMC

Traditional SPICE falls short...

SPICE	Time domain	Frequency domain
Lumped components	Yes	No
Distributed components	No	No

...but ADS can tackle the issues:

ADS	Time domain	Frequency domain
Lumped components	Yes	Yes
Distributed components	Yes	Yes

How to Evaluate ADS

Overview: Three steps

1. Download and install the binaries
2. Request a no-charge 45-day evaluation license
3. Follow the click-by-click demonstration in this Quick Start guide

Step One

Download and install the binaries

- <http://www.keysight.com/find/eesof-ads-latest-downloads>

KEYSIGHT TECHNOLOGIES

Products & Services Technical Support Industries & Technologies About Keysight myKeysight

Home > Products & Services > ... > ADS Simulation Elements > W2301EP Circuit Envelope Element > Software Details

Contact an Expert

Advanced Design System - ADS Software

Choose a platform: Windows Linux Solaris

Current Version Previous Versions

Note: New licenses (v3.2) are required for this release. If you are a supported customer, login to the [Keysight Software Manager](#) to obtain your updated licenses before installation. For other licensing tasks, see ["How to Obtain a License"](#).

Release Date	Version	Version Description
2014-12-11	2015.01	New DDR Bus Simulator, New GoldenGate-in-ADS, New RFIC Cockpit, Silicon RFIC Interoperability w/Virtuoso Enhancements, FEM 2-16x Faster, Layout & Layout Verification Improvements, numerous other usability, performance and productivity improvements

Free Trial Available

How to Download

- [Downloading Your Keysight EEsof EDA Software](#)

Download Installs on: PC

How to Install Operating System

If you get stuck at any time, click here and Keysight expert will help you

Step Two

Request a no-charge 45-day evaluation license

- <http://www.keysight.com/find/eesof-ads-evaluation>

KEYSIGHT TECHNOLOGIES myKeysight United States

Request Free Trial License

What's New in KSM?

1 Assign Licenses 2 Contact Information 3 Review and Submit

Assign licenses to hosts, then click Continue to proceed. [Help](#)

Select the host to assign licenses to

Enter new host information: [How do I find my Host ID?](#)

Valid CPU IDs:

- server cpu id (7-10 hex characters)
- mac address (12 hex characters- no spaces. Example: 123456abcdef)
- hardware key (9-1234abcd or 10-1234abcd)
- hardware key (8- followed by 12 hex characters - no spaces)

CPU ID :

You may enter one or three CPU IDs (separated by a space).

Select the licenses to assign

<input type="checkbox"/>	License	Version	Quantity Available	Quantity to Assign
<input checked="" type="checkbox"/>	W2200F-1U1-TRL ADS Evaluation License - floating	N/A	1	<input type="text"/>

Step Three

Follow this hands-on demonstration

– Go to:

<http://edadocs.software.keysight.com/display/eesofkcads/Workshop+on+Including+Parasitic+Inductance+Effects+on+DC-DC+Converters>

..and download the archived ADS workspace (as shown below) to the “home folder” that you picked during ADS installation:

The screenshot shows the Keysight Knowledge Center interface. At the top, there is a search bar and navigation links. The main content area displays the article title "Workshop on Including Parasitic Inductance Effects on DC-DC Converters". Below the title, there is an "Issue" section and a "Solution" section. The "Solution" section contains the text "This workspace provides detailed exercises that show how ADS can simulate undesired transient signal degradation in DC-to-DC converters due to parasitic inductances. They are targeted at users who have little or no experience using ADS." A red box highlights the word "workspace", and a blue callout box points to it with the text "Right click here to download the *.7zads archive to your ADS home folder".

Note: If you didn't receive a Knowledge Center login with the demo license, please register now

KEYSIGHT TECHNOLOGIES

Login

Accessing this service requires you to log in.

Login Name (Email):

Password:

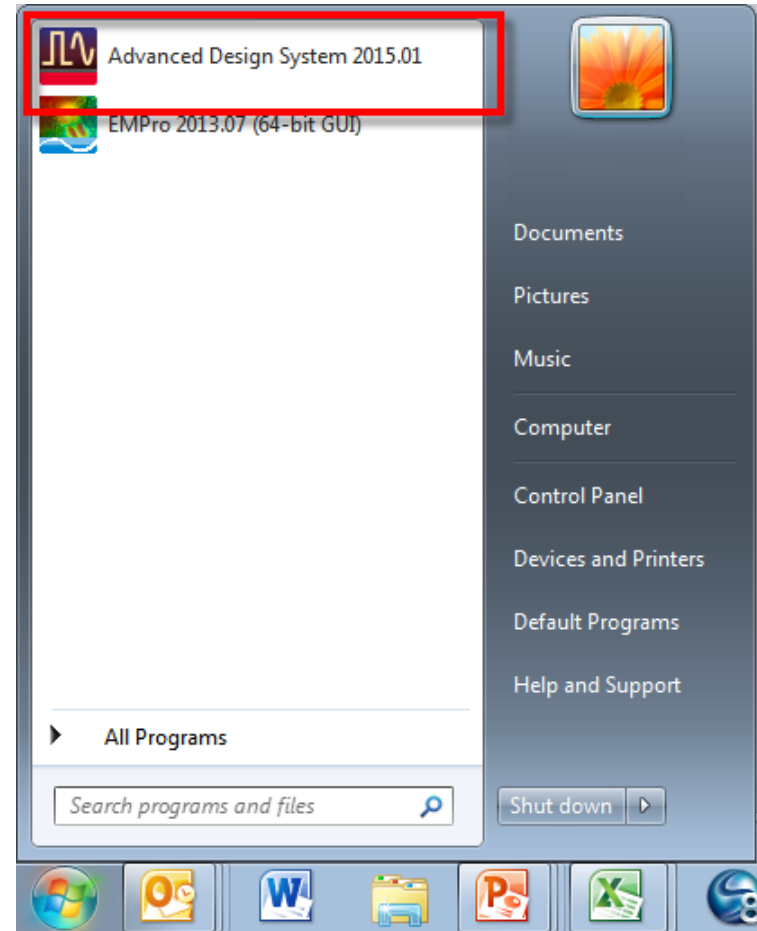
Login **Cancel**

If you don't already have a Knowledge Center login, register by clicking here

- ▶ Don't have a Login Name? [Register](#)
- ▶ [Reset Password](#)
- ▶ If you are unable to log in, please [reset your password](#). We have recently updated our site.
- ▶ Having login problems? [Contact Webmaster](#)

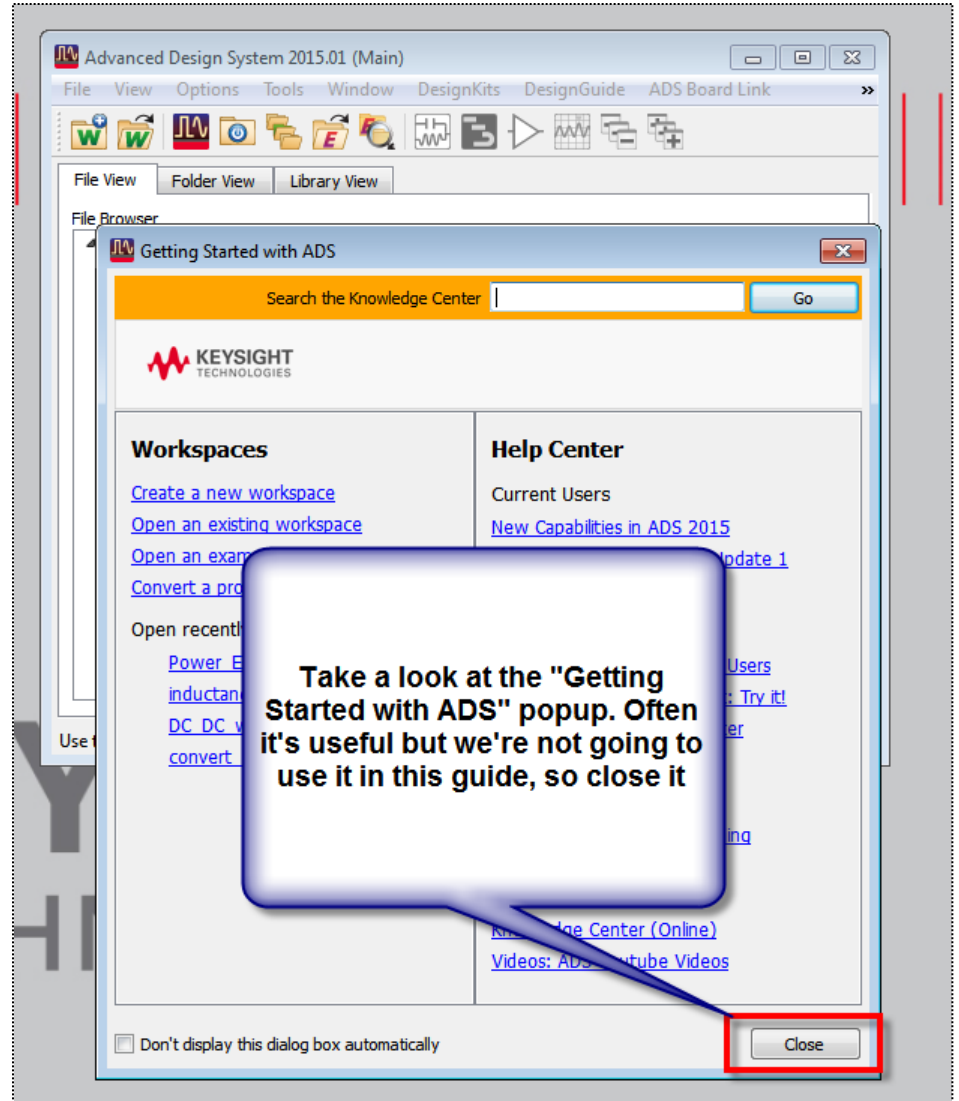
Start Advanced Design System

– Start → Advanced Design System



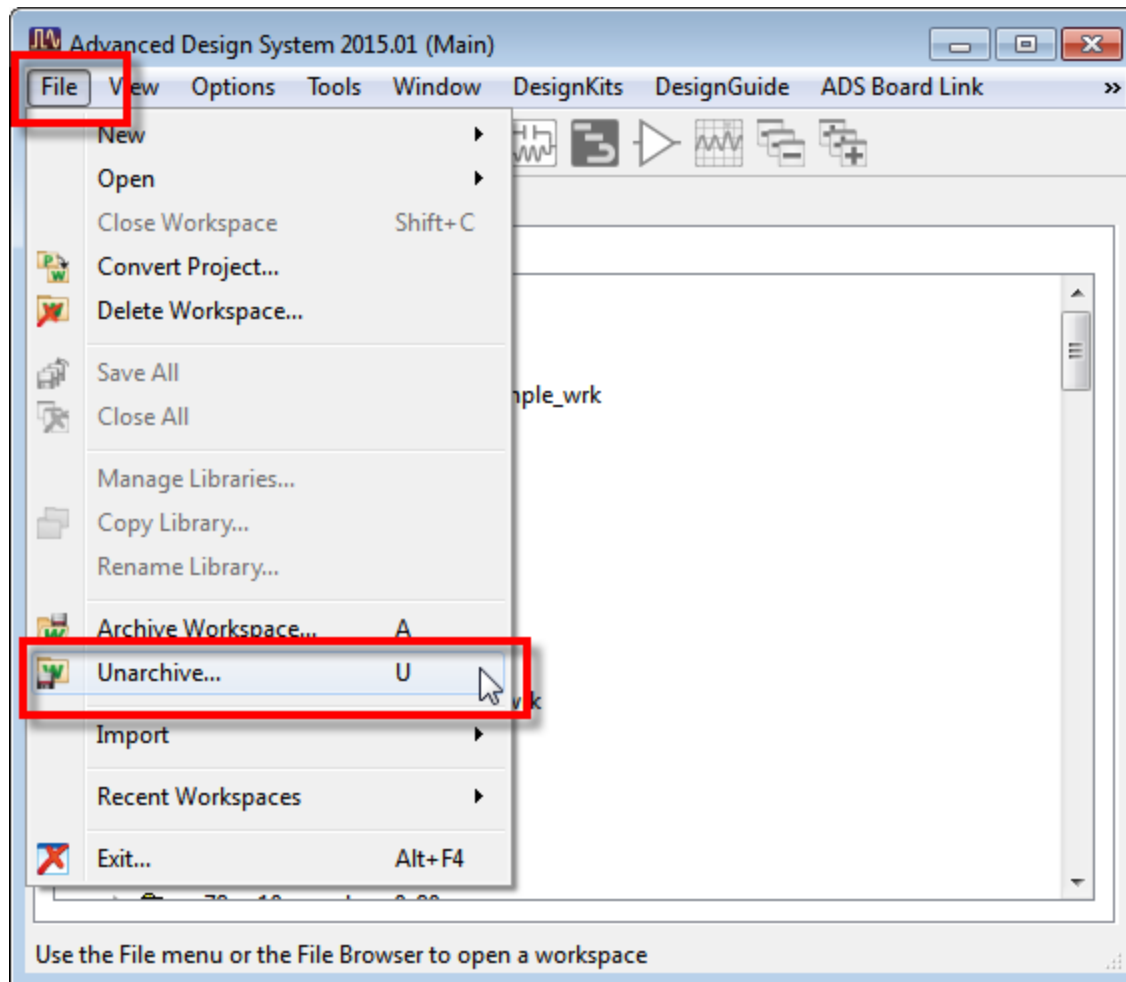
Two windows open...

- ...examine but then close the "Getting Started with ADS" popup window



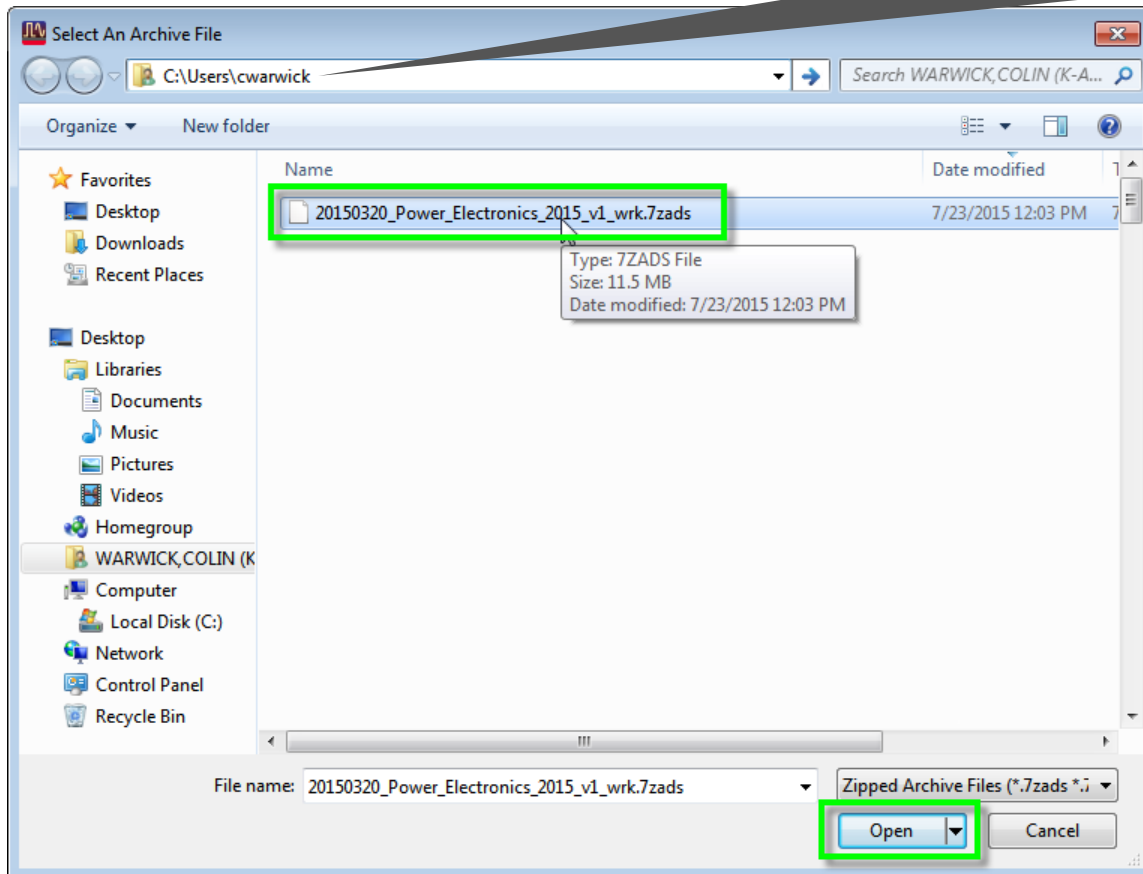
The ADS “Main” window remains...

From the Main window menu bar, select the *File* → *Unarchive...* dialog box



Select and open the *.7zads archive you downloaded

I downloaded the archive to C:\Users\cwarwick. Of course, you'll need to navigate to the folder you picked.



This guide doesn't cover the principles of operation but our YouTube video "How to Design DC-DC Convertors" has a refresher if you need one.

How to Design DC-to-DC Converters

Keysight EEs of EDA
"How to" Video

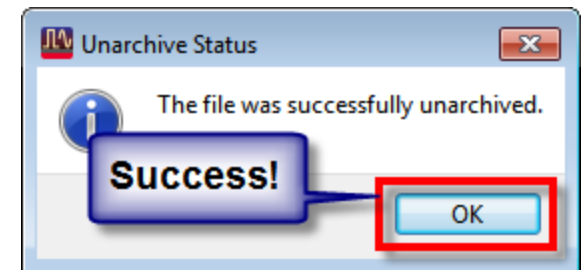
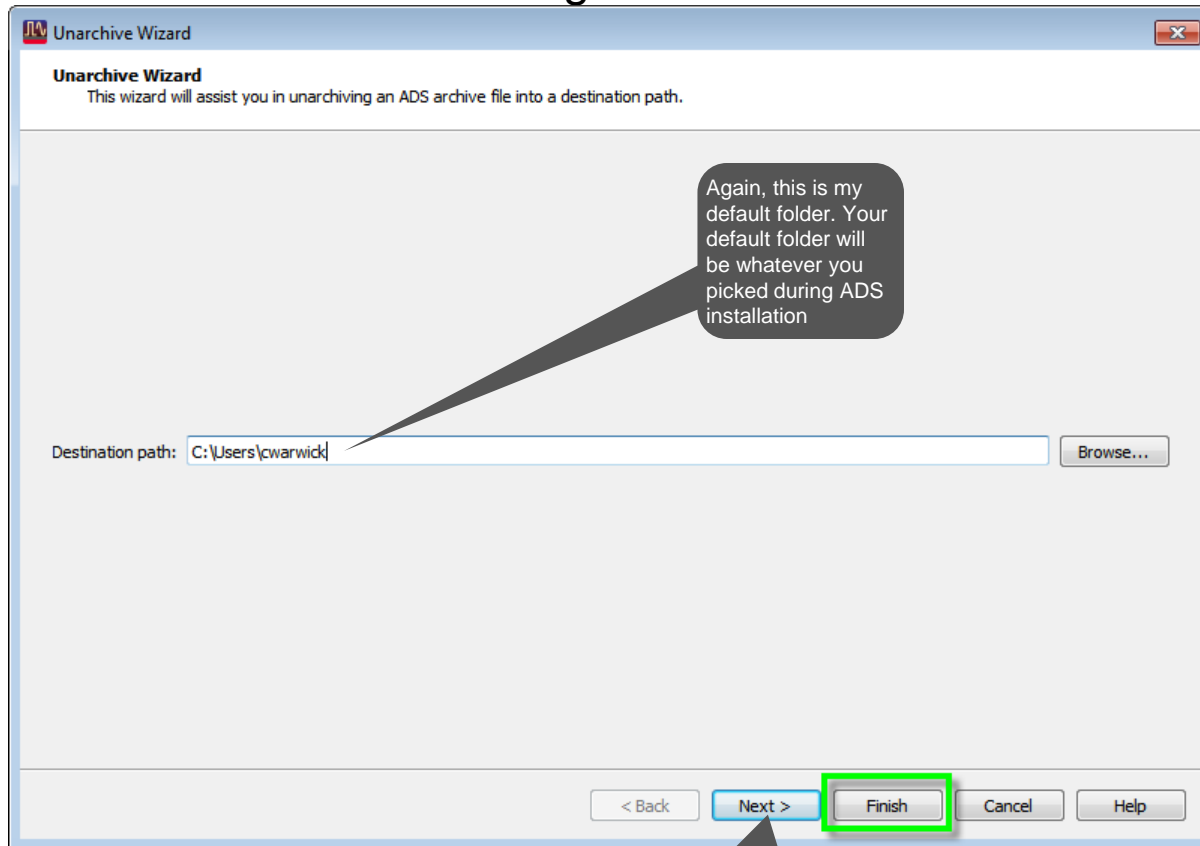
Andy Howard
Applications Engineer
Keysight EEs of EDA

DOWNLOAD
YOUR NEXT
↓INSIGHT

KEYSIGHT
TECHNOLOGIES

Accept the default settings of the Unarchive Wizard

- Ignore the “Next” button and just click the “Finish” button to accept all the default settings



Close the Readme window, leaving "Main" open

The screenshot displays the Advanced Design System 2015.01 (Main) interface. The top window, titled "Advanced Design System 2015.01 (Main)", shows a hierarchical folder view of the workspace. The folder structure includes:

- 1. Exercise 1 - Voltage Drop Due to Parasitic Inductance
- 2. Exercise 2 - Surge Voltage
- 3. Exercise 3 - Noise variation with Capacitor Placement
- 4. Exercise 4 - Gate Surge
- 5. Exercise 5 - Inductance Estimation
- 6. Exercise 6 - Momentm EM Simulations
- 99. Subcircuits
- A_Readme
- laminat
- laminat.dds
- substrate1_v1.subst
- substrate1.subst
- substrate2.subst
- temp1.subst

Two callout boxes provide instructions:

- The default view into the workspace is a hierarchical "Folder view"** (pointing to the folder list).
- You can close the Readme window for now** (pointing to the 'A_Readme' folder).

The bottom window, titled "A_Readme [Power_Electronics_2015_lib:A_Readme:schematic] (Schematic):1", shows a schematic editor. A callout box states:

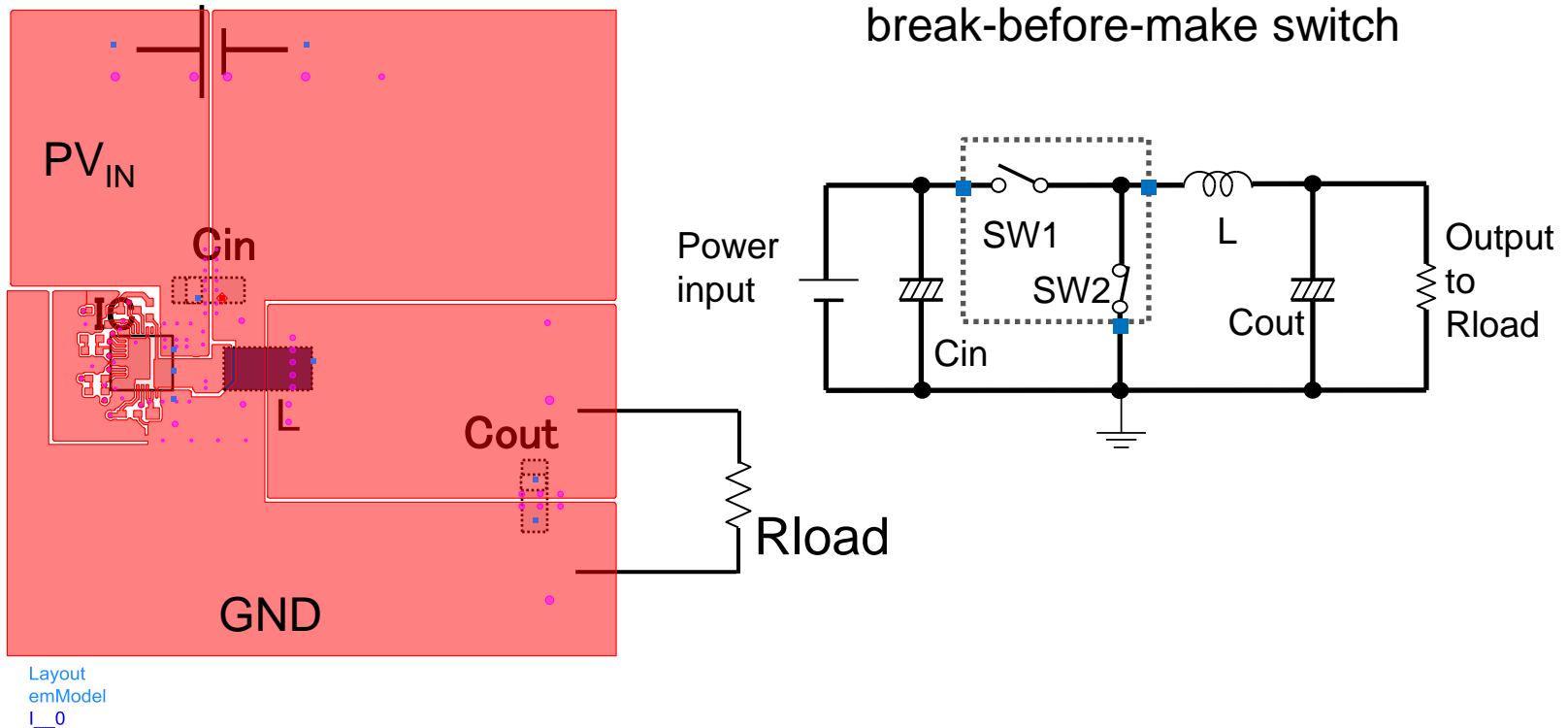
- You don't need this PDF at the moment** (pointing to the schematic area).

Below the callout, blue text reads:

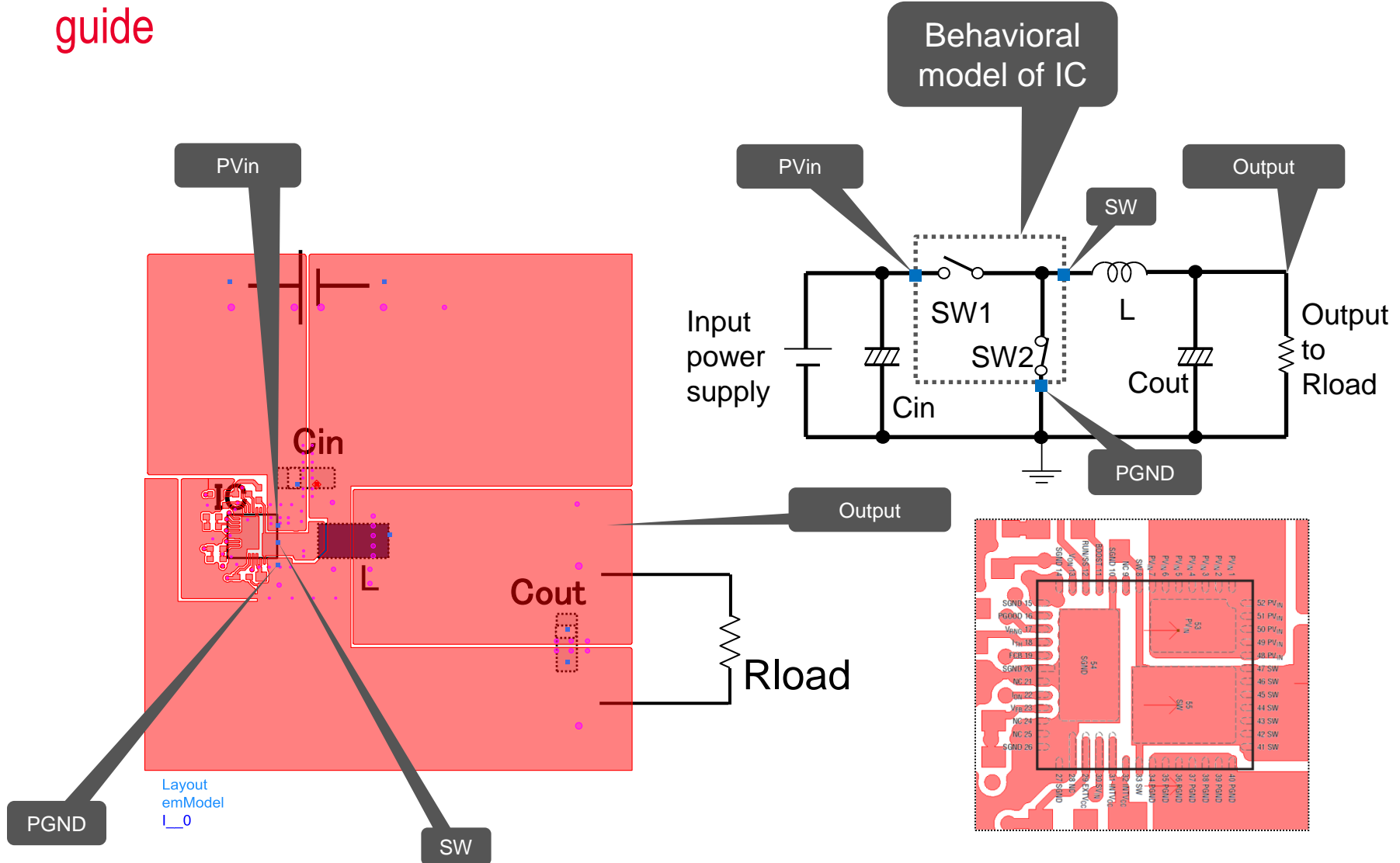
For details about this workspace, refer to the [Power_Supply_Workshop.pdf](#) document inside this workspace's directory.

We are going to model a switch-mode DC-DC convertor. Here's a simplified version...

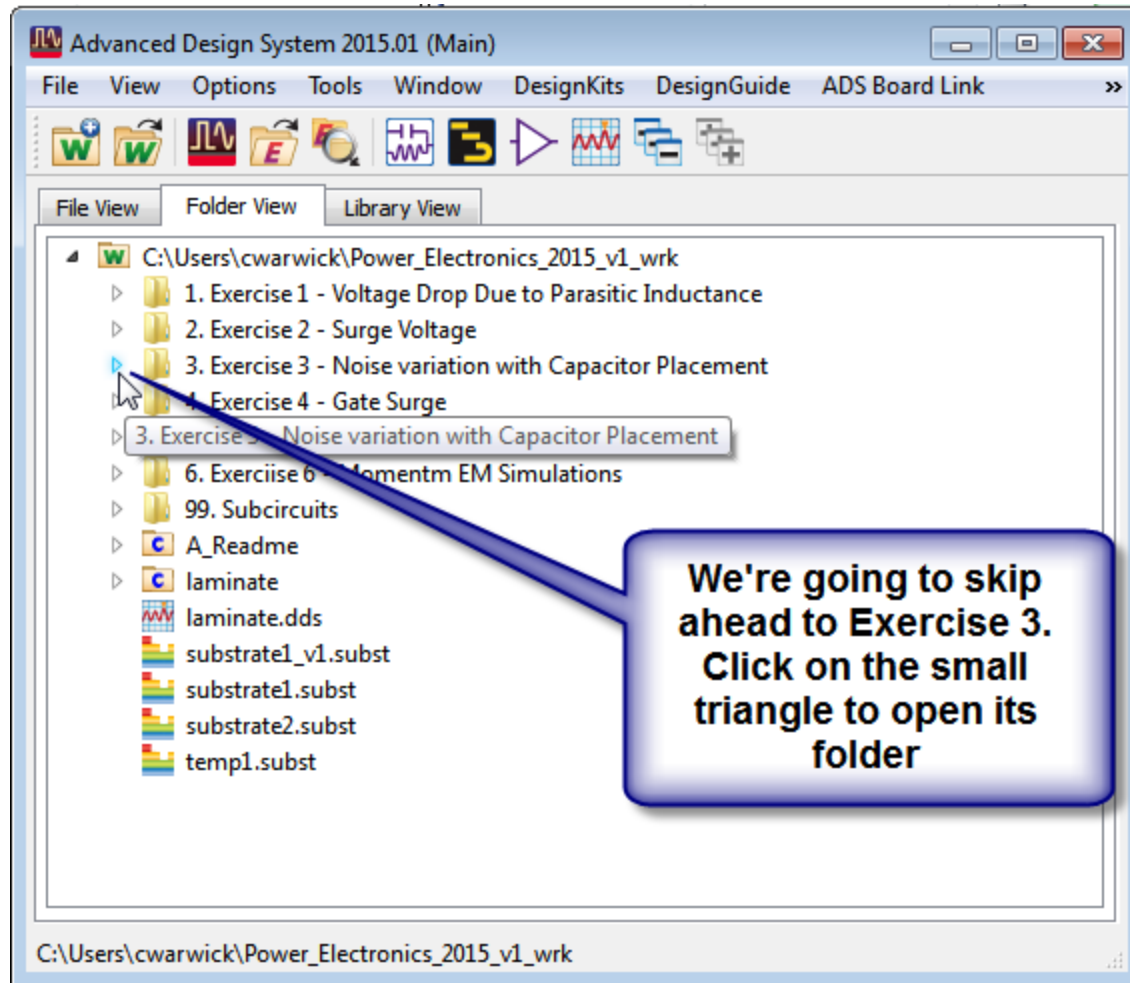
We are going to model the IC behaviorally as a simple single-pole, double-throw, break-before-make switch



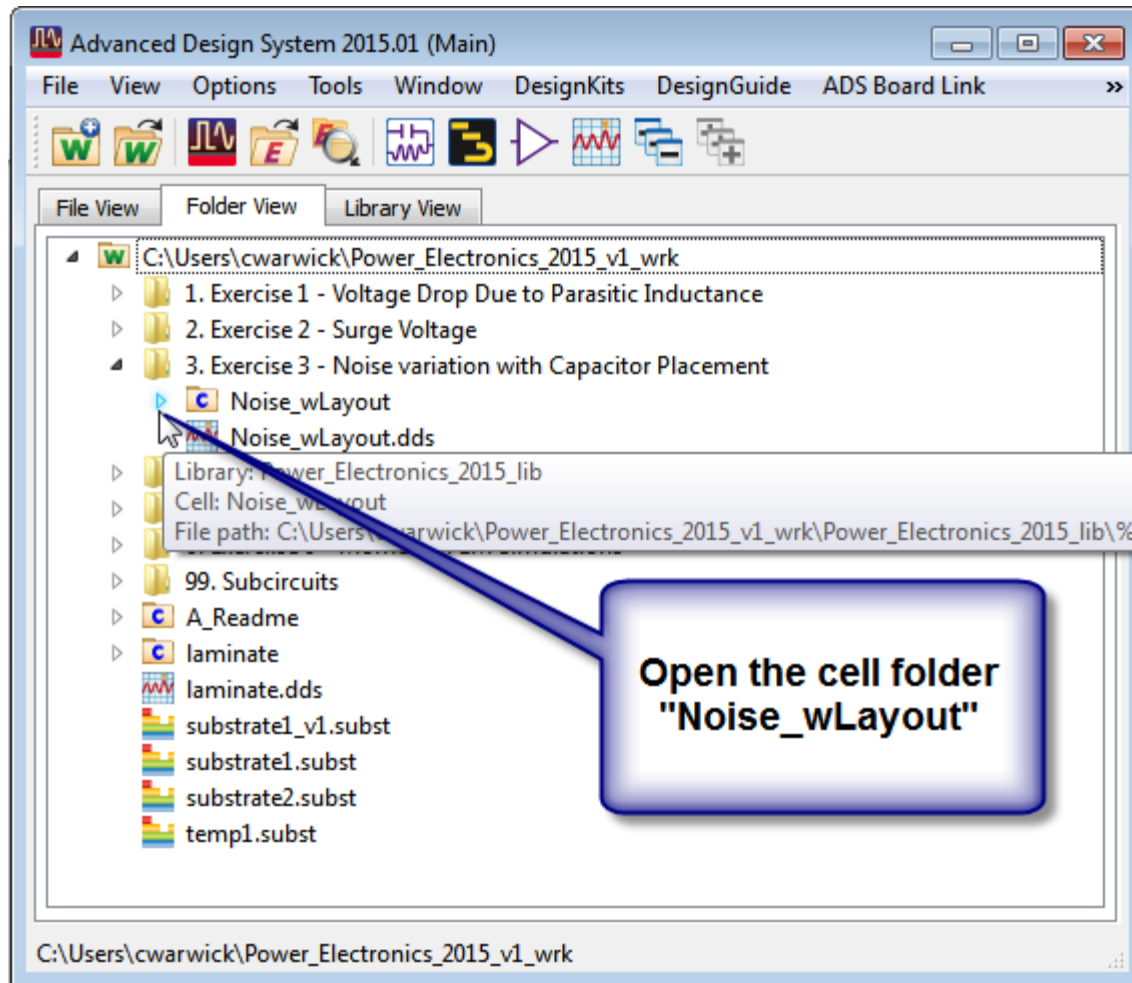
Side note: The actual IC is LTC3609 from Linear Technology, but we don't need the full vendor model for the purposes of this guide



Let's see the real thing: Open the Exercise 3 folder



Open the cell folder "Noise_wLayout"



Side note: Multi-technology in ADS

Skip this slide if you like and come back to the idea later

- A **Workspace** contains one or more **Technology Libraries**

Q. Why would you want multiple technologies? A. For example, chip, package, and board can have their own Technology Library, each with their own namespace, stack up, component library, PDK, etc.

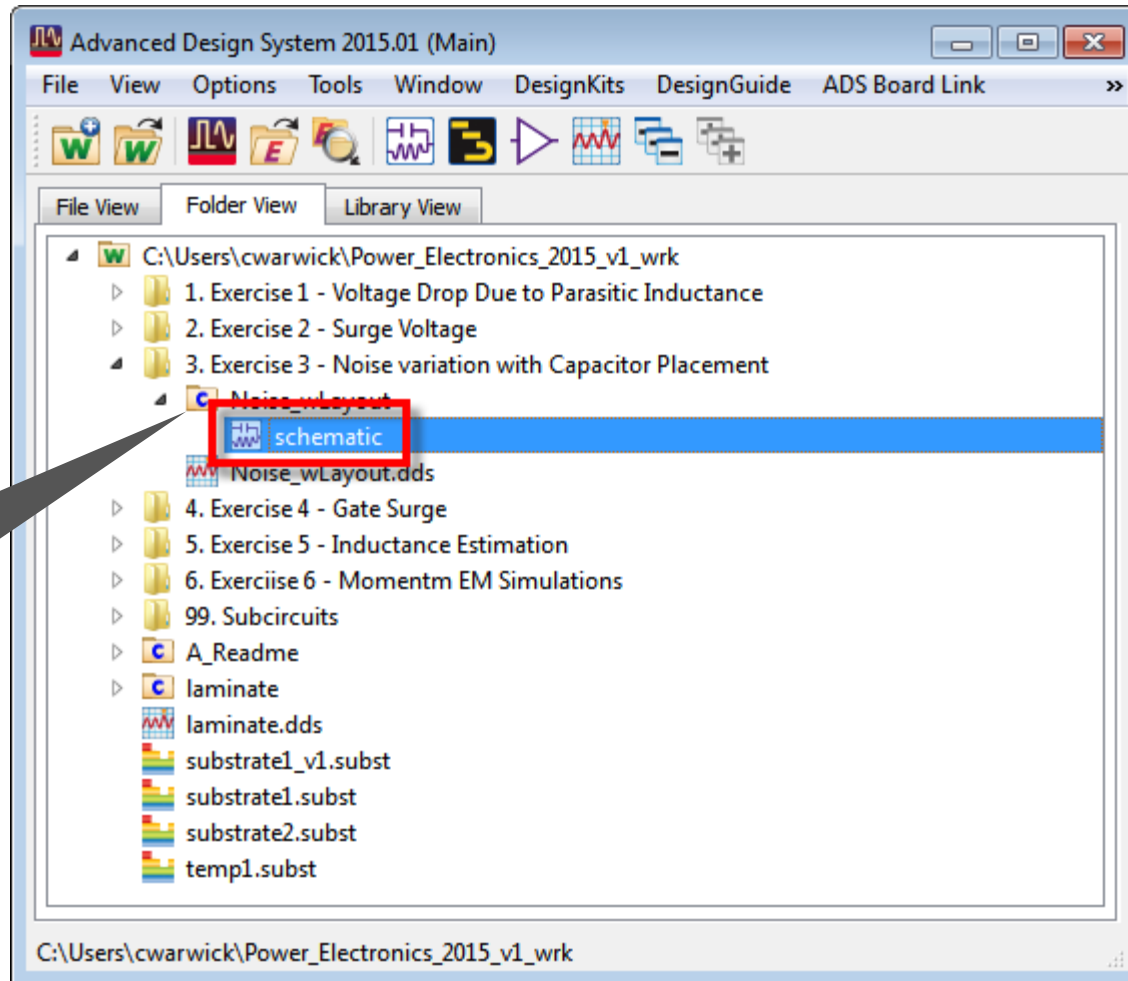
- A **Technology Library** contains one or more design units (subcircuits), called “**Cells**”

Q. Why would you want more than one? A. You might want hierarchy e.g. subcircuit cells instantiated on a top-level circuit cell. You can even instantiate a cell from one tech. library inside of a cell from another. For example, to place a chip in a package, and a package onto a PCB, just like the real world.

- A **Cell** can be viewed in one or more ways, called “**Views**”

Q. What are the names of some Views? A. The “black box” view is called “Symbol view”, the circuit view is “Schematic”, the flat physical view is “Layout view”, the perspective physical view is called “3D layout view” and so on

Double click on “schematic” view of the Noise_wLayout cell



Folders that contain Cells and Views of the Cell have a letter “C” on them

There is a lot going on here, so maximize the window, and let's take a quick tour...

The screenshot displays the Keysight circuit simulation software interface. The main window shows a schematic diagram of a power electronics circuit. A callout box with a blue border and white background points to the maximize button in the window's title bar, containing the text "Maximize the window".

The circuit schematic includes a DC voltage source labeled "Vdc=12 V" connected to a switch "SWITCHV1" and "SWITCHV2". The circuit also features two diodes, "DIODE1" and "DIODE2", and a load resistor "R1 R=0.4 Ohm". A transient analysis is configured with the following parameters:

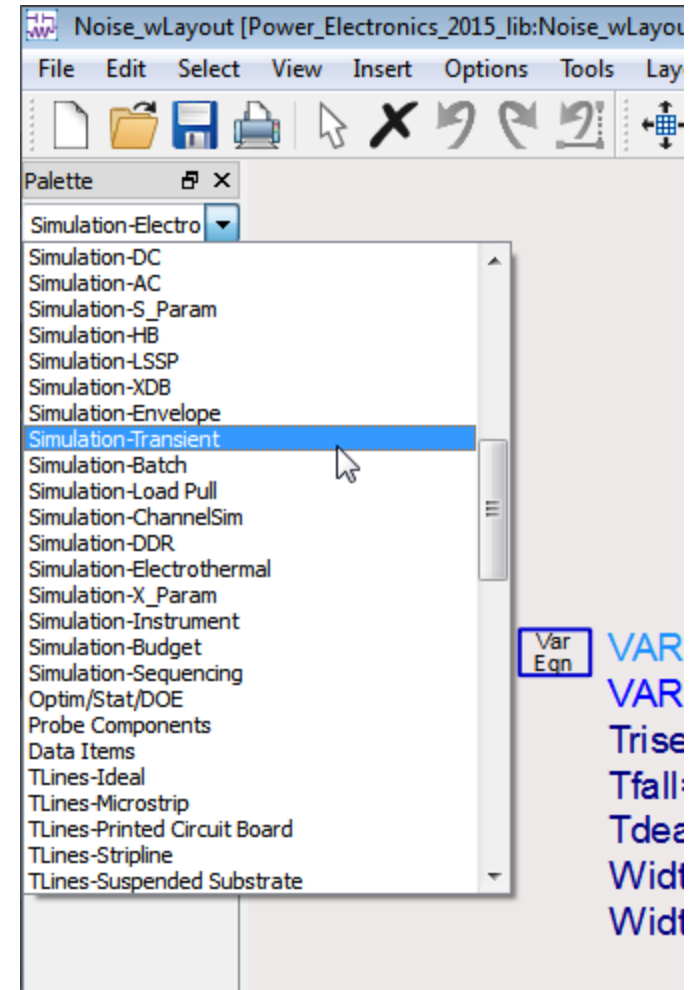
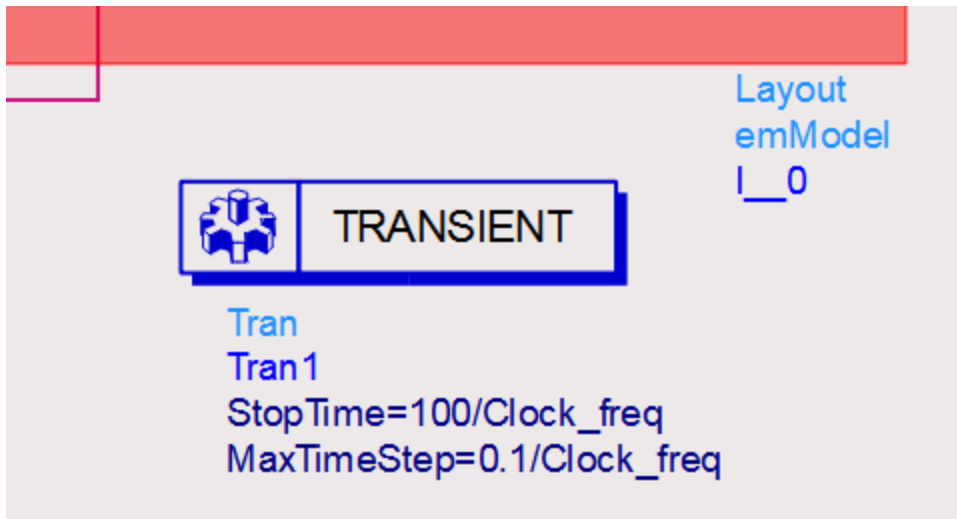
- Tran1
- StopTime=100/Clock_freq
- MaxTimeStep=0.1/Clock_freq

The software interface includes a menu bar (File, Edit, Select, View, Insert, Options, Tools, Layout, Simulate, Window, DynamicLink, DesignGuide), a toolbar, and a component palette on the left. The palette lists various components such as resistors (R, R_Model), inductors (L, L_Model), capacitors (C, C_Model), and diodes (DIODE1, DIODE2). The status bar at the bottom indicates "0 items" and "ads_device:drawing -0.250, -3.125 in".

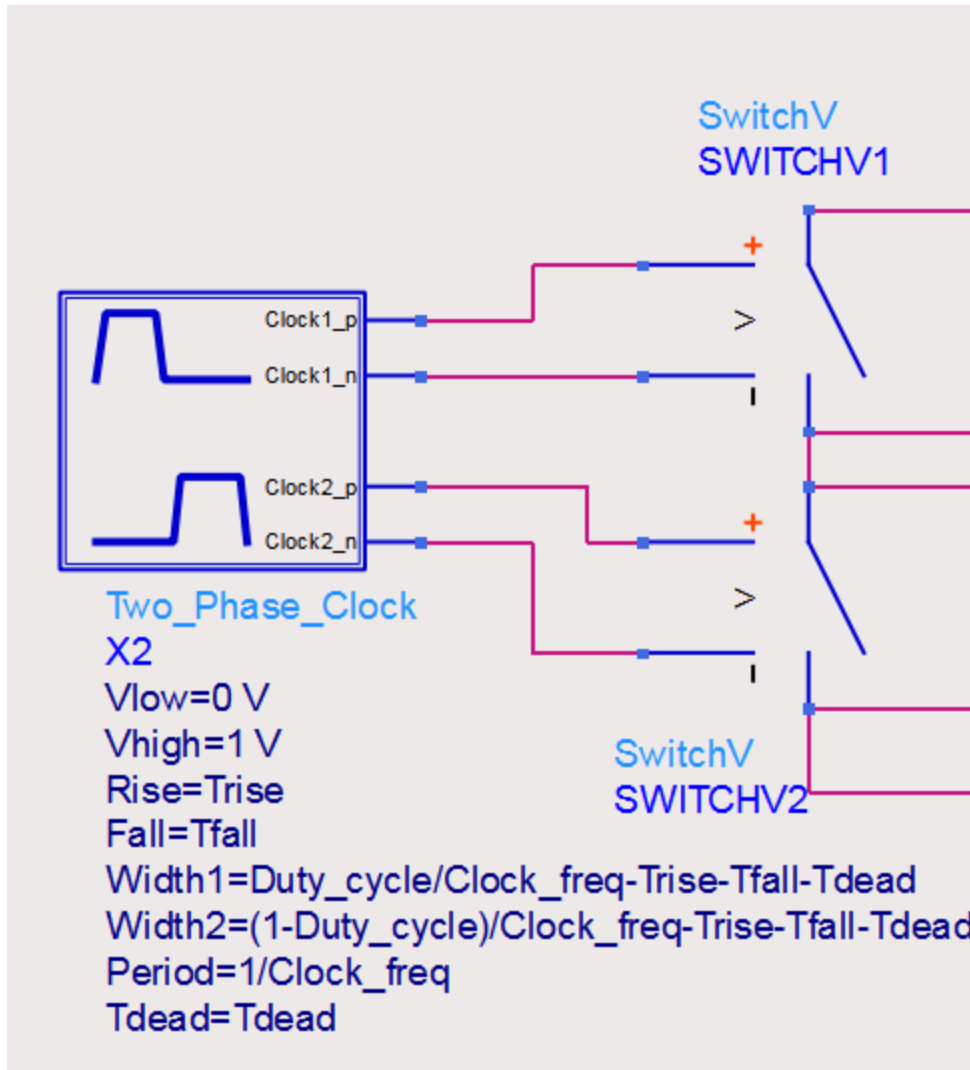
The top-level schematic has a simulation controller

- In this particular case we are using the time-domain SPICE-like simulator in ADS called “Transient”
- It includes a Convolution engine so it is sometimes called “Transient Convolution” or just “TC”

Note: Transient is just one of many circuit simulators available for ADS...

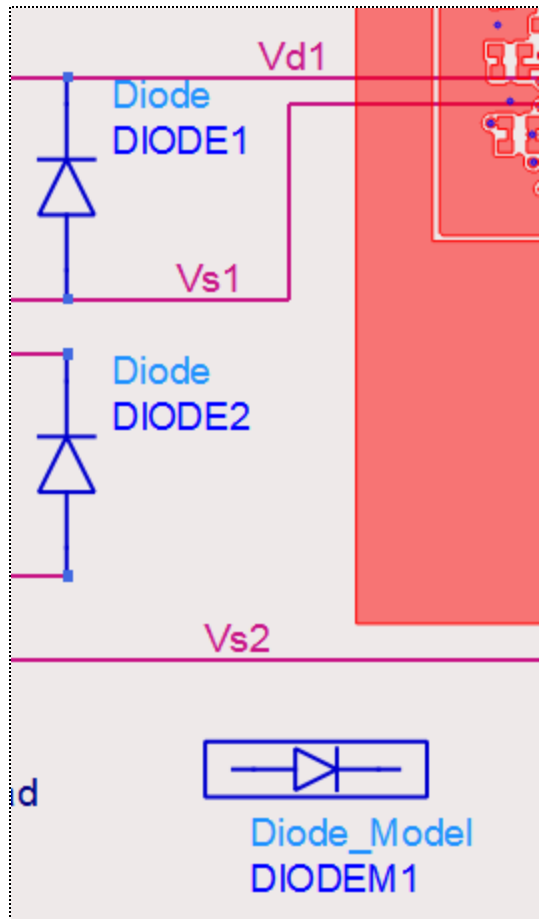


Components can be modelled behaviorally...



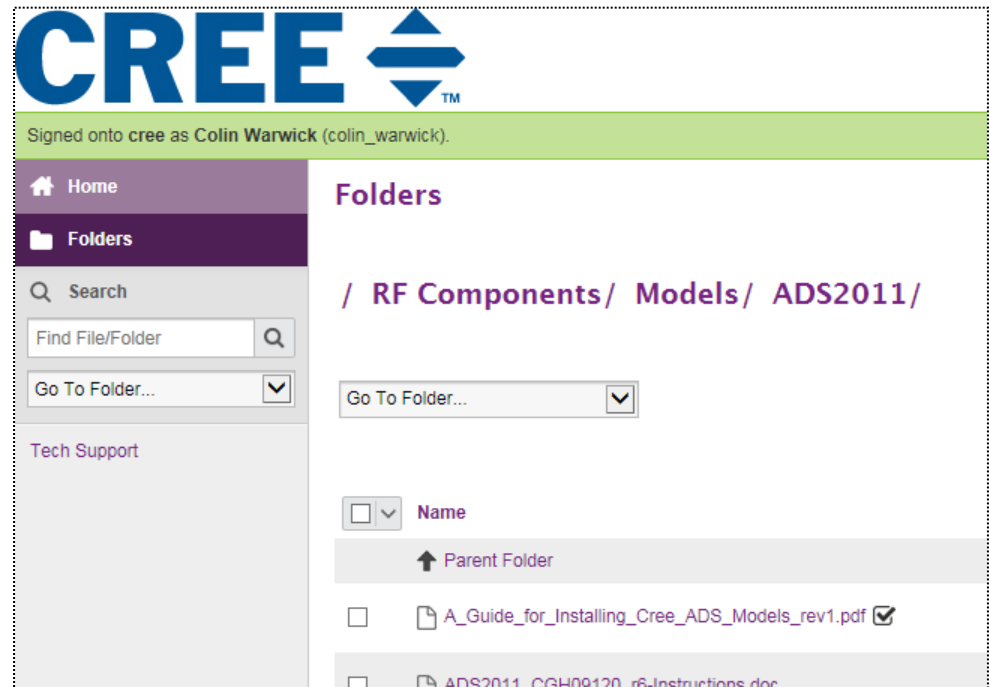
In this guide we model the IC as an ideal single-pole, double throw, break-before-make switch

...or using physics-based, vendor-specific “model cards”



Note: Not used in this guide, but many microelectronic vendors offer models for ADS. For example, Cree:

<http://www.cree.com/RF/Tools-and-Support/Model-form>



VAR blocks contain expressions evaluated *before* the simulation runs

- Can be convenient for parameterization, especially for parameter sweeps

```
Var Eqn VAR VAR2
Trise=100 nsec
Tfall=Trise
Tdead=50 nsec
Width1=Duty_cycle/Clock_freq-Trise-Tfall-Tdead
Width2=(1-Duty_cycle)/Clock_freq-Trise-Tfall-Tdead

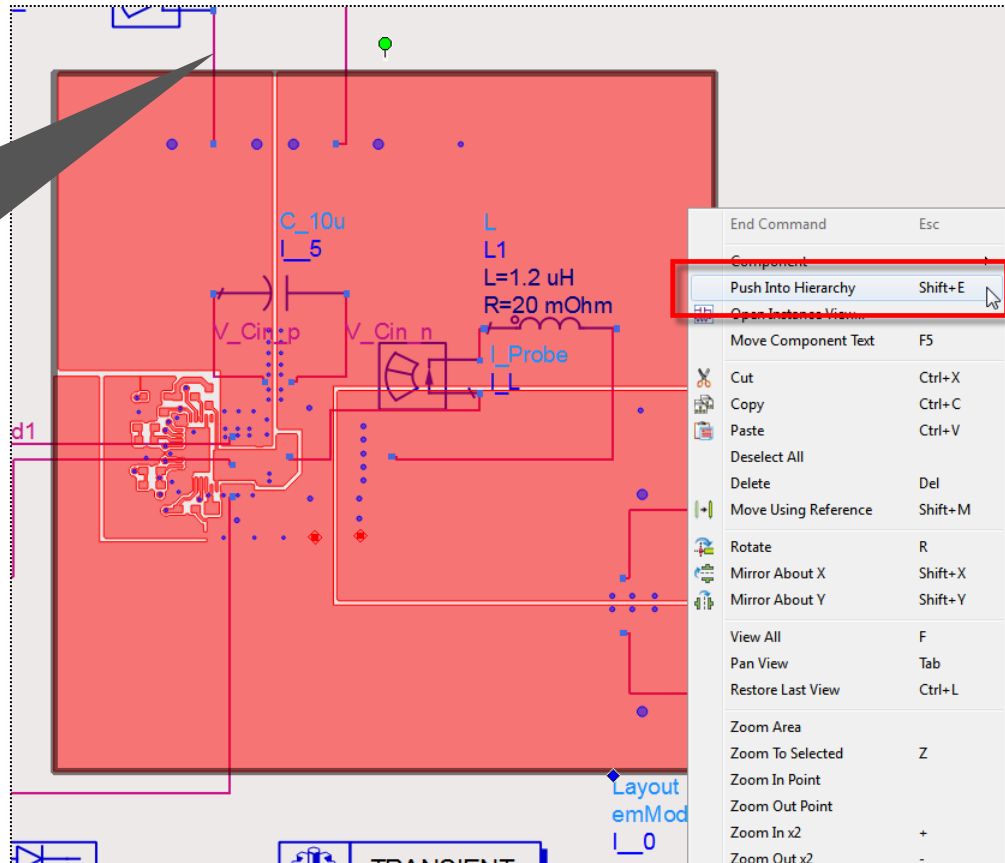
Var Eqn VAR VAR3
Clock_freq=500 kHz
Duty_cycle=0.30
```

Note: ADS also has EQN or Measurement Equation blocks, which are similar to VAR blocks, but contain expressions that are evaluated *after* the simulation has run. Useful for analysis of simulation results, waveforms etc.

Most important: the “Look-alike” component

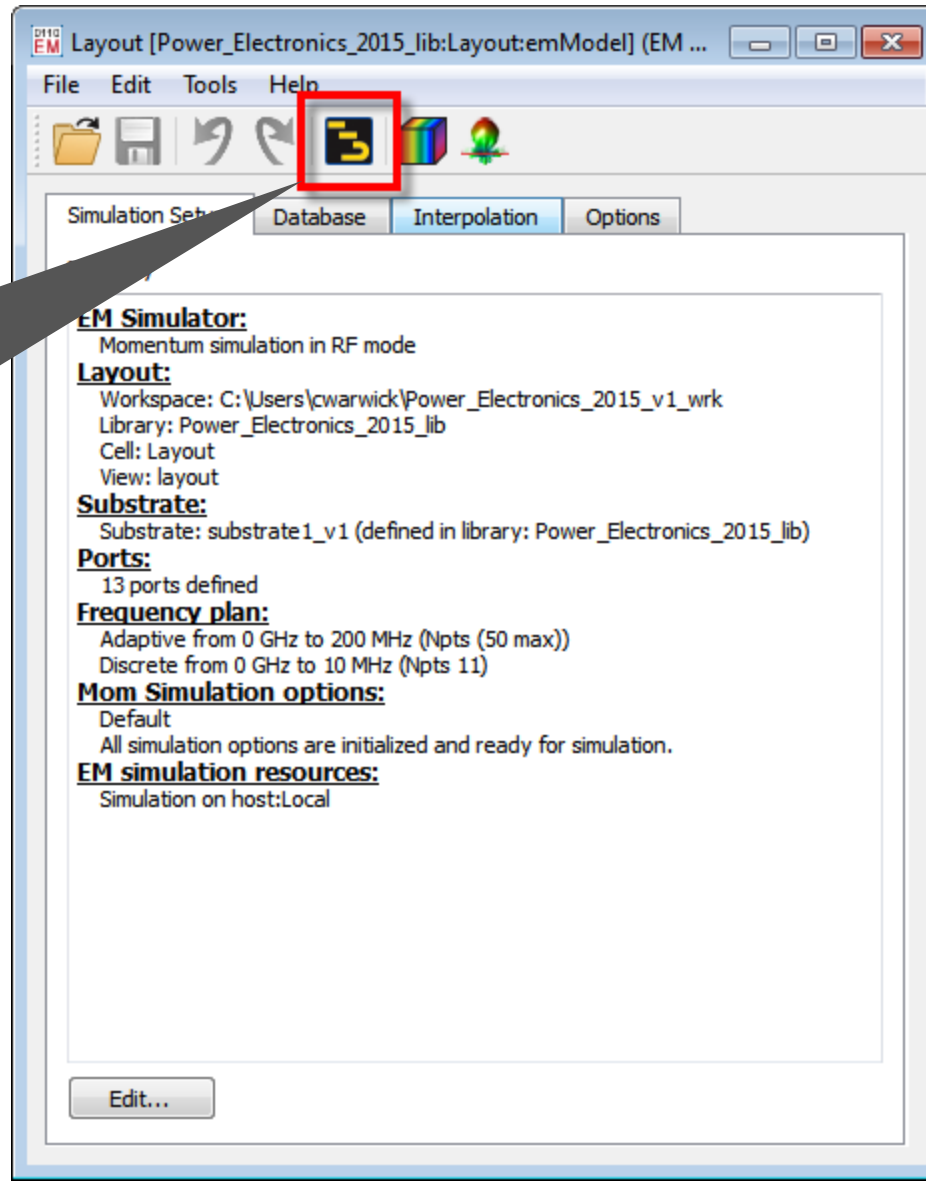
The EM field solver in ADS can extract a model of the layout parasitics! Right click on it and select “Push into Hierarchy” from its popup context menu

Note: The connection between the lumped component and the distributed component is represented by a magenta line with a blue square at each end

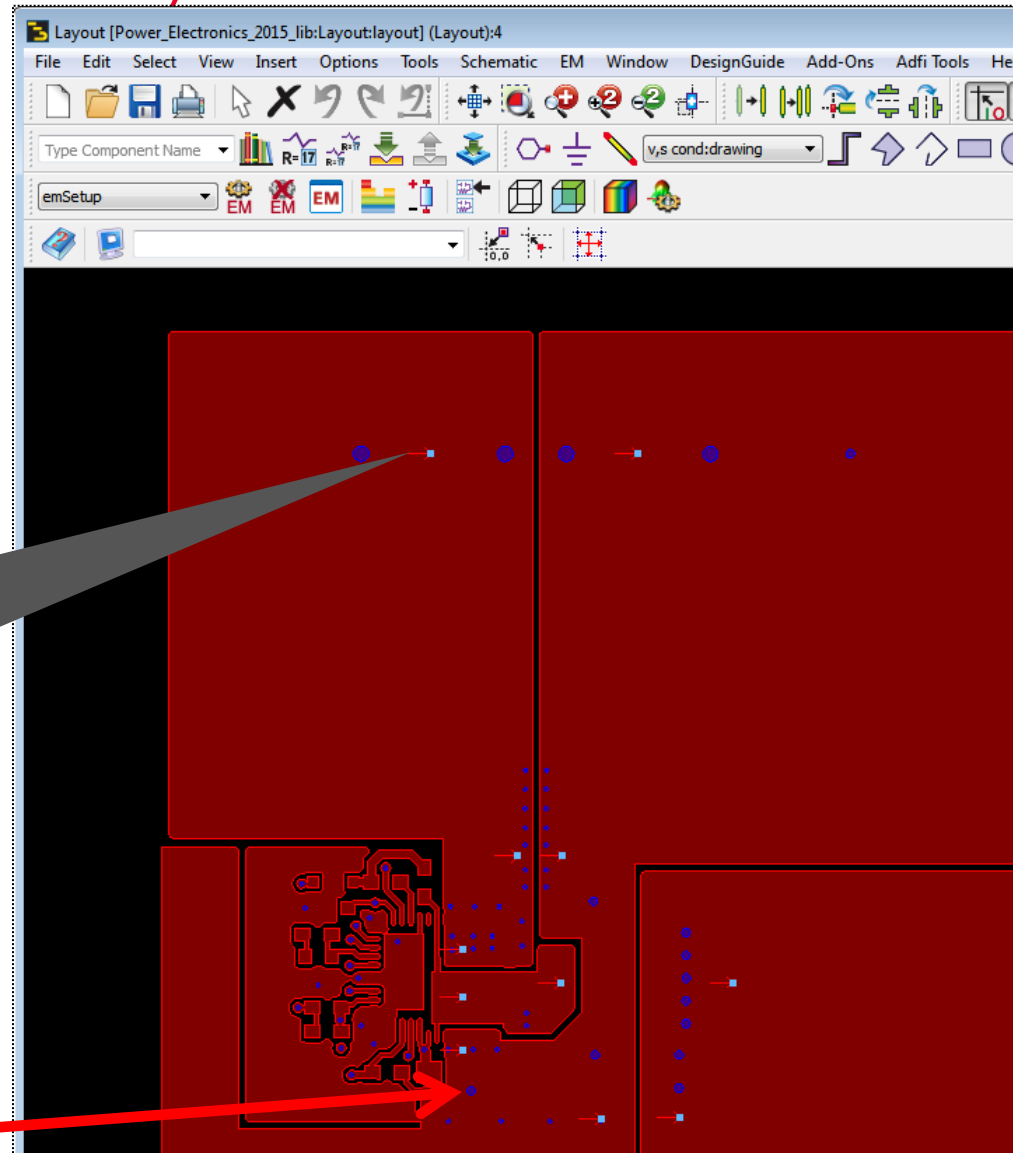


Under the hood are details of the EM model.
Click on the layout icon to open the artwork

Opens the
layout view
of the cell
called
"Layout"



The EM model is based on 1) the actual PCB artwork...



Note: In layout view, a "pin" is represented by small cyan square with a red arrow coming out

The dark blue circles are via holes

...and 2) the material properties of the stackup of the technology library that the layout is in

Layout [Power_Electronics_2015_lib:Layout:layout] (Layout):4

File Edit Select View Insert Options Tools Schematic EM Window DesignGuide

Type Component Name v,s cond:drawing

emSetup

Substrate Editor

Opens the substrate of the current EM setup in the editor.

substrate1_v1 [Power_Electronics_2015_lib] (Substrate):5

File Technology View Options Tools Window Help

Substrate Name: substrate1_v1

Use right mouse context menus to add or delete substrate items.
Select items on the substrate and view their properties below.

Conductor Layer

Layer art002 (40)

Material Cu

Operation Sheet Intrude into substrate Expand the substrate

Position Above interface Below interface

Thickness 35 micron

Angle 90 degrees

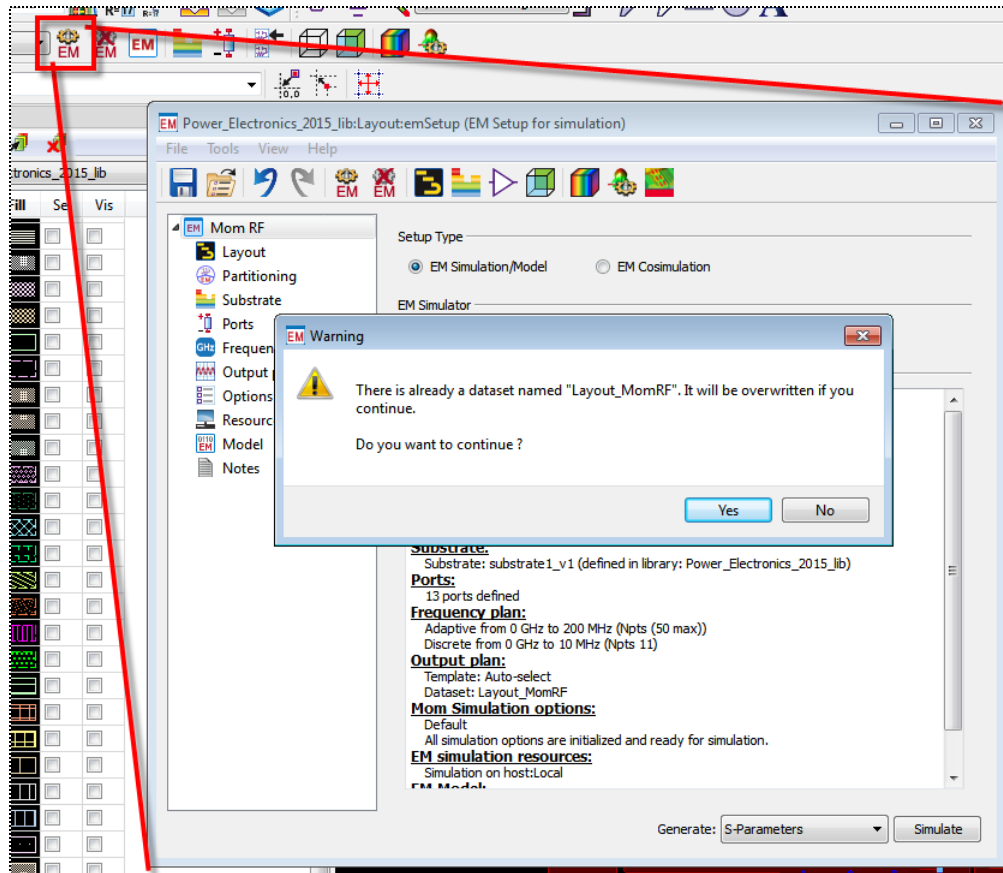
Surface roughness model Top <None> Bottom <None>

Precedence 0

To move the conductor up or down on the substrate, just drag it up or down.

Layer	Material	Operation	Position	Thickness	Angle	Surface roughness model
art001	Cu	Sheet	Above interface	35 micron	90 degrees	<None>
art002	Cu	Sheet	Above interface	35 micron	90 degrees	<None>
art003	Cu	Sheet	Above interface	35 micron	90 degrees	<None>
art004	Cu	Sheet	Above interface	35 micron	90 degrees	<None>
Dielectric_1	Dielectric_1	Intrude into substrate	Below interface	0.3 millimeter		
Dielectric_1	Dielectric_1	Intrude into substrate	Below interface	0.3 millimeter		
Dielectric_1	Dielectric_1	Intrude into substrate	Below interface	0.3 millimeter		
AIR	AIR	Expand the substrate	Above interface	10 millimeter		
AIR	AIR	Expand the substrate	Above interface	10 millimeter		

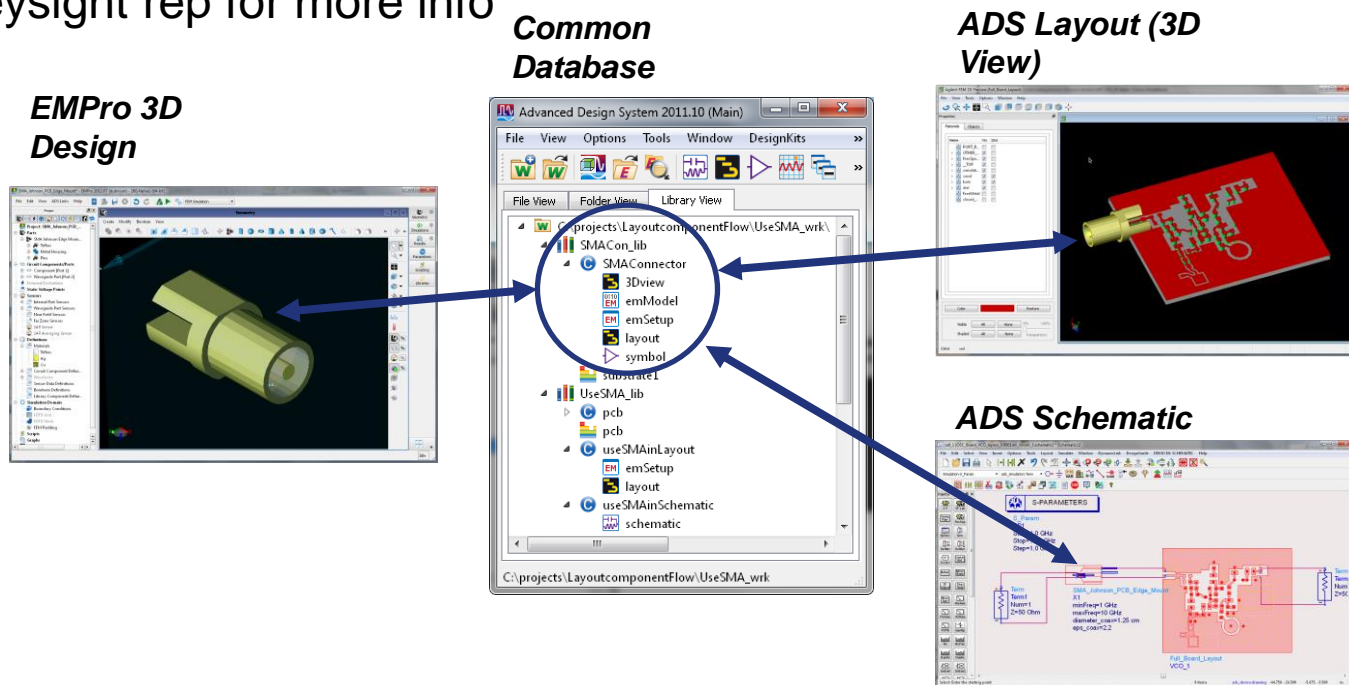
Optional: Click the EM cog icon, and click “Yes” to re-build the EM model dataset



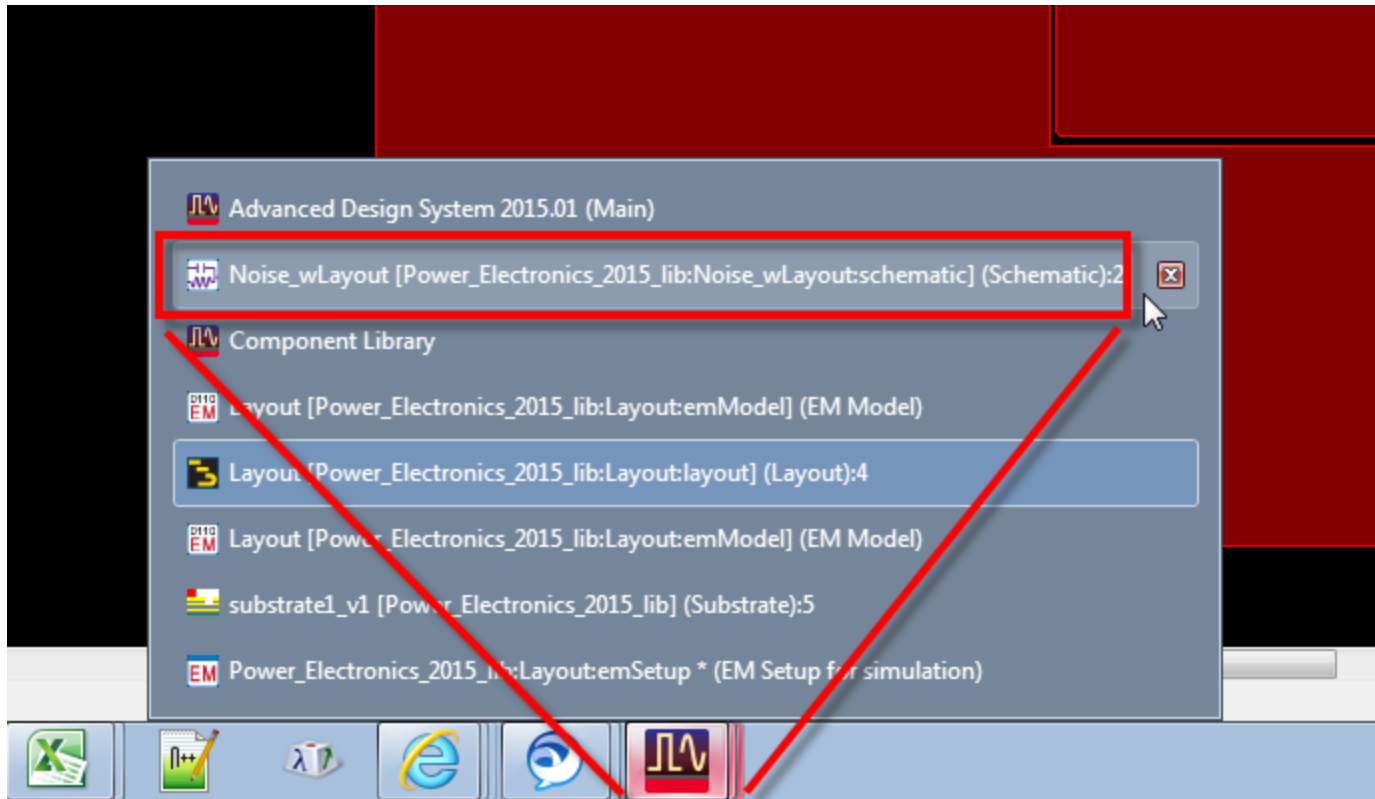
Caution: If you perform this optional step, the EM simulation takes about 20 minutes on a typical PC. This step is optional because we already ran the EM simulation for you and saved the resulting dataset in your workspace.

Side note: The EMPro add-on to ADS can build EM models of arbitrary 3D shapes like magnetics and integrate them with layout and schematic

- Advanced topic: not covered further in this guide
- Contact your Keysight rep for more info



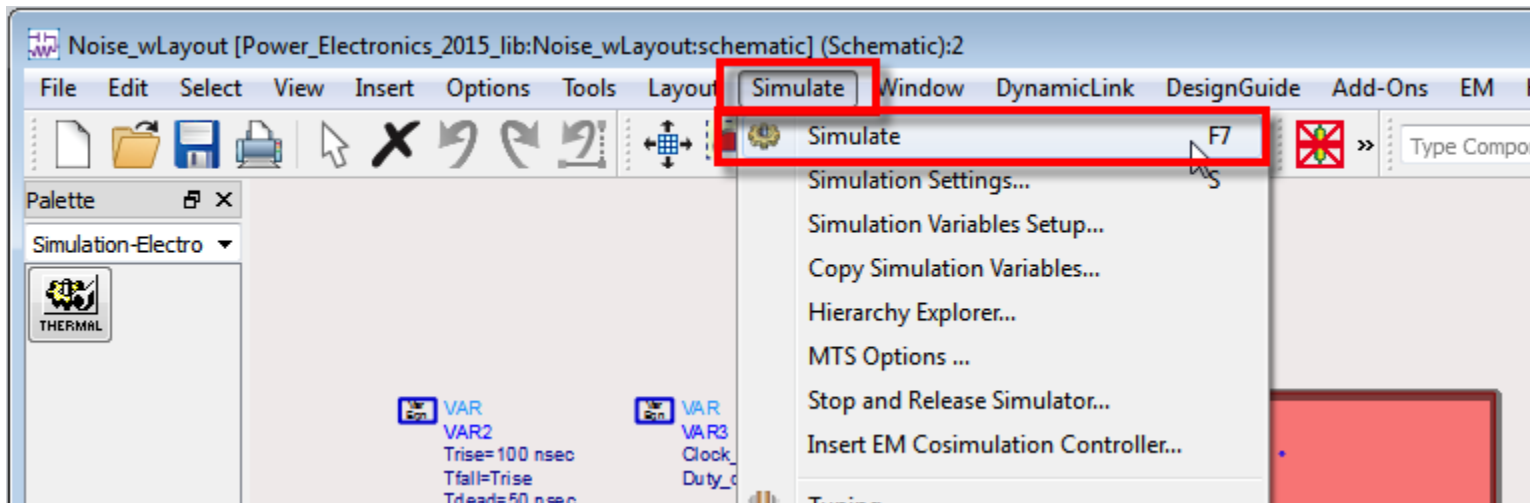
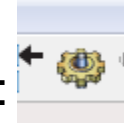
From the Windows task bar, bring the original schematic back on top



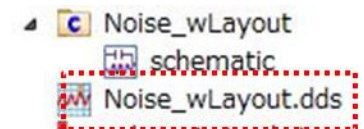
From the schematic menu bar, select Simulate → Simulate

Note: You could also:

- 1) Use the F7 hotkey or
- 2) Click the simulate (cog wheel) icon in the tool bar:



After a few seconds, the simulation finishes, and the data display window opens automatically...



Side note: The *.dds file extension means “data display server”

Rescale the Y-axis in the baseline ripple plot

...in preparation for comparing this "good" design with the "bad" one that we'll do next

The load voltage increases while Switch1 is on (and the inductor current is increasing) and decreases while Switch2 is on (and the inductor current is decreasing.)

83.94 m

2.179

2. Select the "Plot Options" tab

3. Select "Y axis"

4. Uncheck "Auto Scale"

5. Set Min=2.10, Max=2.35, Step=0.05

6. Click "OK"

1. Double click any white space on the plot canvas to open the "Plot Traces & Attributes" dialog box

Y-axis label: Cycles

Y-axis ticks: 3.5, 4.0, 4.5, 5.0, 5.5, 6.0, 6.5, 7.0, 7.5

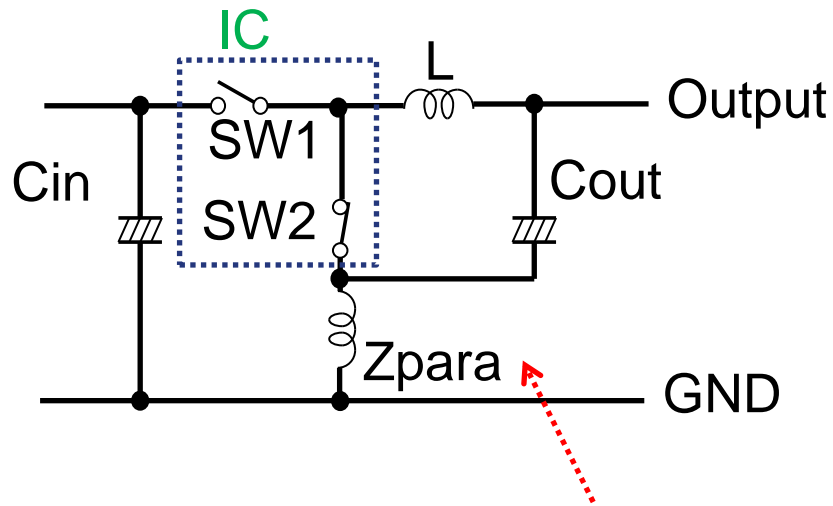
X-axis ticks: 196.0, 196.5, 197.0, 197.5, 198.0, 198.5, 199.0, 199.5, 200.0

Plot Traces & Attributes dialog box settings:

- Plot Type: Linear
- Select Axis: Y Axis
- Axis Label: (empty)
- Auto Scale:
- Min: 2.14
- Max: 2.24
- Step: 0.02

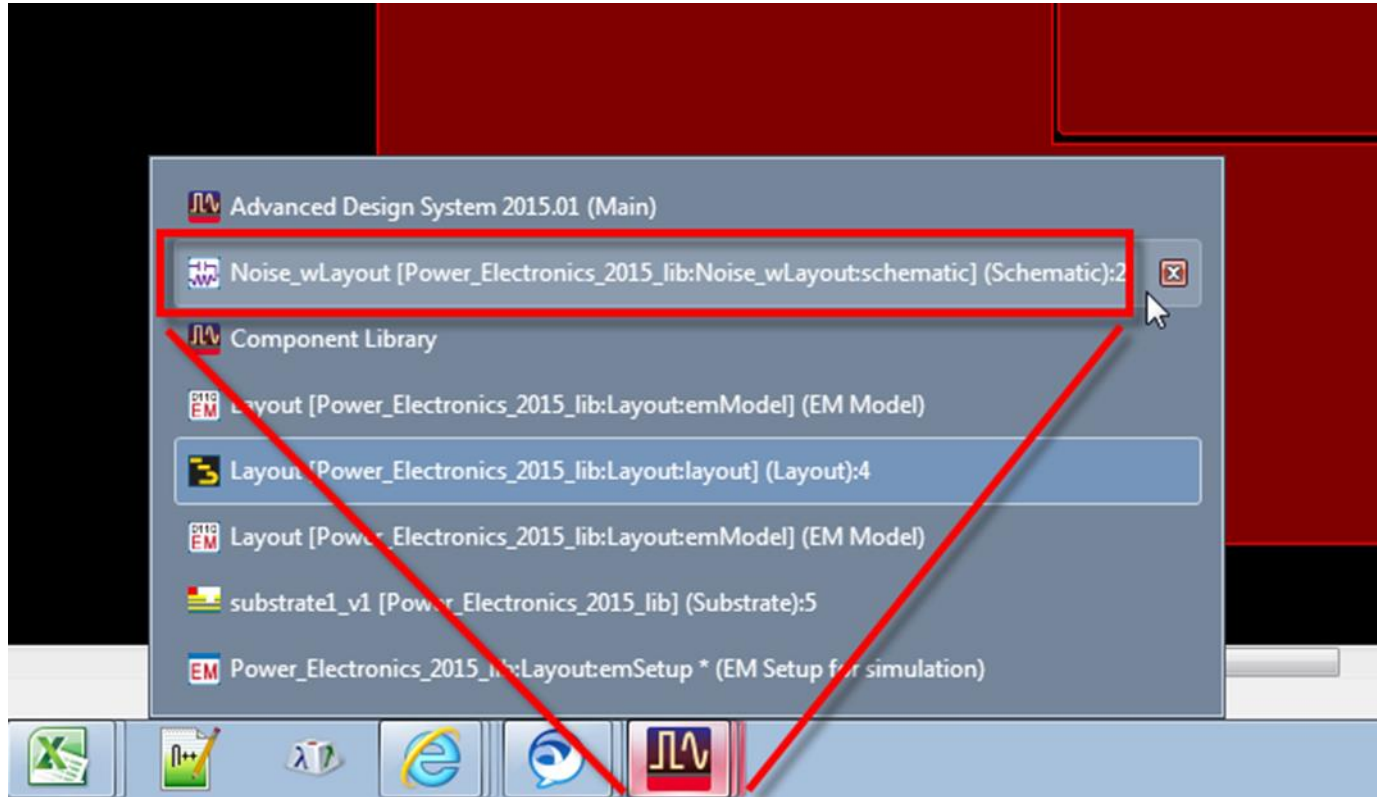
Next let's see the effect of layout parasitics on ripple...

Parasitic impedance causes more ripple noise



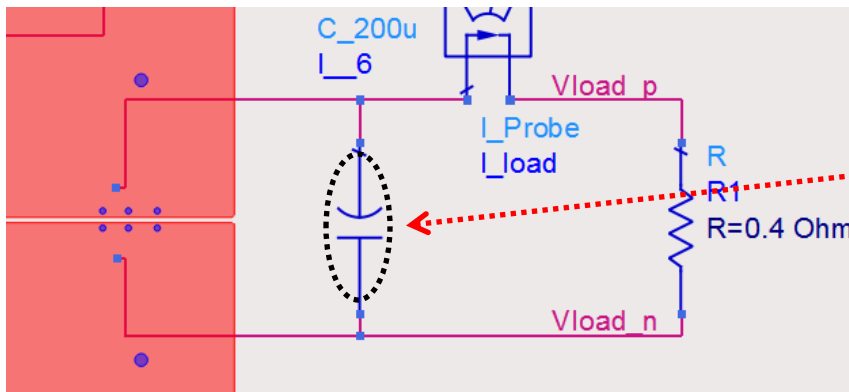
Let's show what happens to ripple if we add a parasitic impedance by artificially increasing the trace length between C_{out} and the output ports to R_{load}

Bring the schematic window back on top

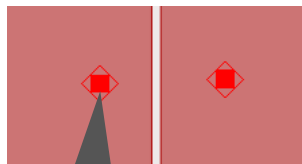


We are going to change the connection points of C_200u (Cout)

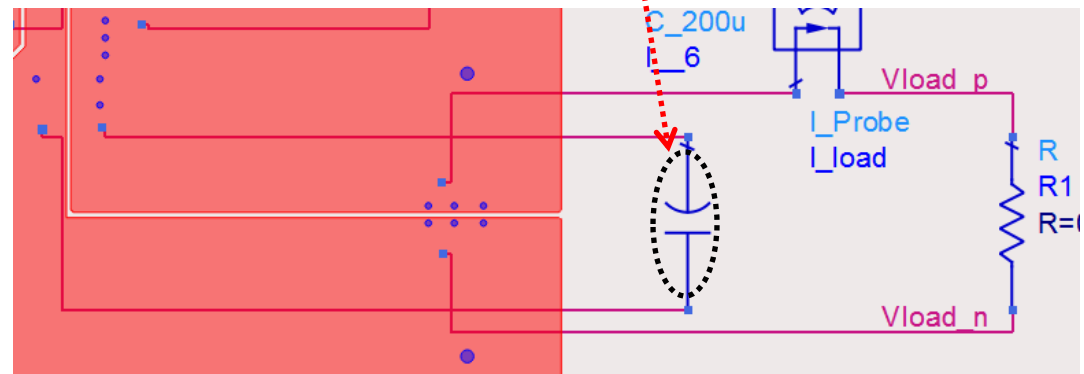
Exact steps are on the next slide...



Change in placement on the PC board

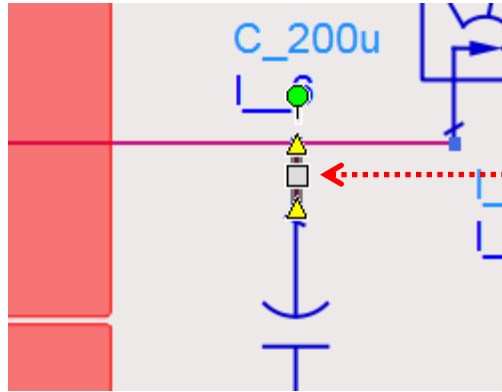


Note: Before you connect them, pins are red diamonds




How to change the connection points

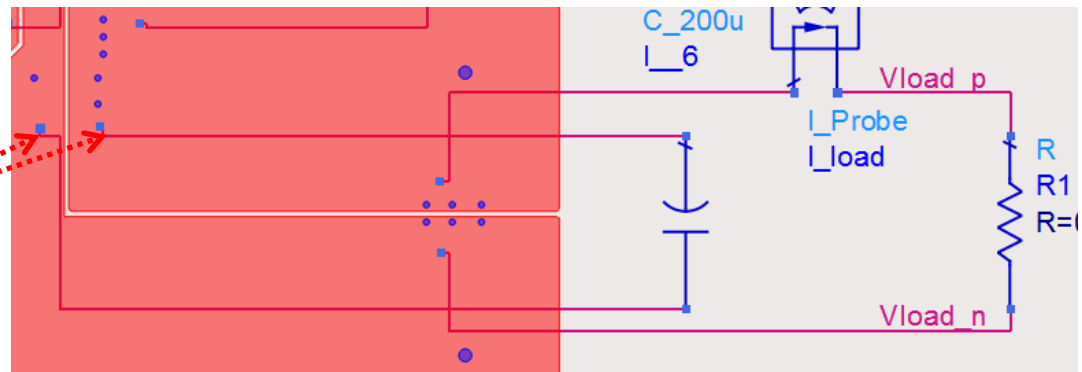
1. Left click to select the wire. Next, hit the Delete key. Remove the other wire connecting C_200u.




Left click here. Then press the “Delete” key. Repeat for the bottom net.

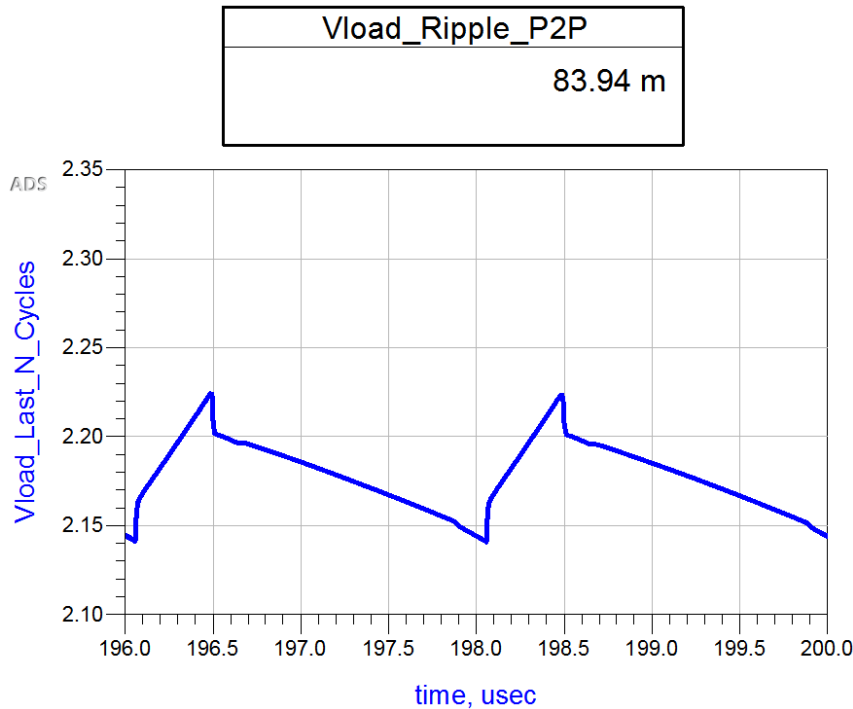
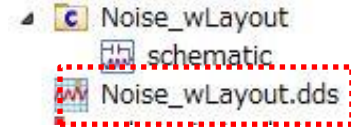
2. After clicking , left click on the nodes as shown to re-connect the capacitor.

New port connections

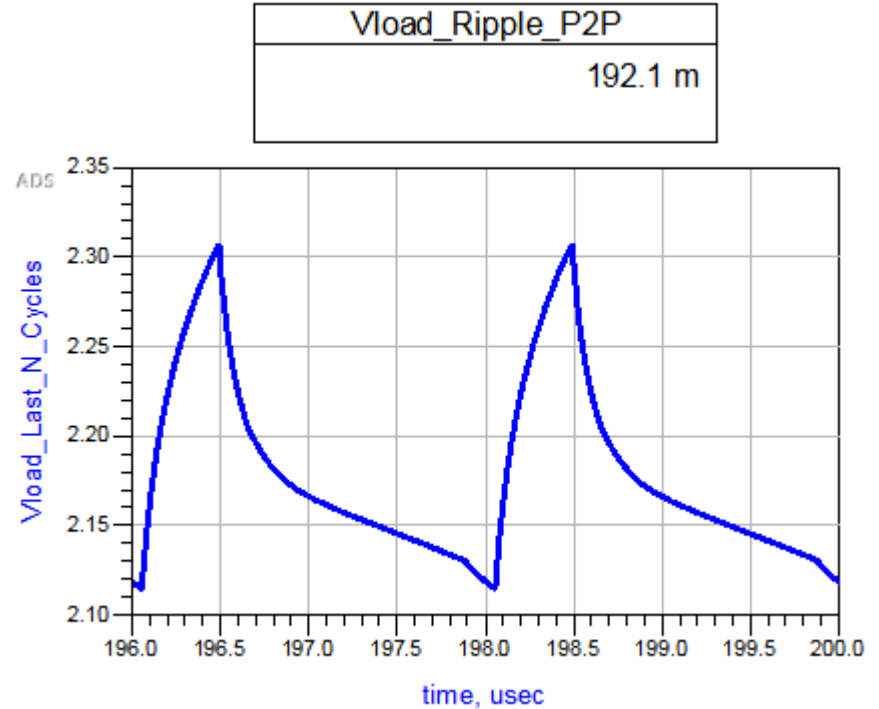


Re-run with “bad” connection points

Click  to re-run the simulation. The “display dataset” window comes into focus again.



Before: Low layout parasitic



After: High layout parasitic

Note: Do Y-axis scaling on the new plot as before

Conclusion and Next Steps

In power electronics, ADS can solve problems that SPICE alone cannot

This guide has just a small taste! Contact your Keysight EEsof EDA expert for further e-learning material to meet your needs!

<http://www.keysight.com/find/eesof-support>

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hours: 8:00am - 8:00pm ET, Mon - Fri

address: P.O. Box 4026
Englewood, CO 80155-4026
United States

SPICE	Time domain	Frequency domain
Lumped components	Yes	No
Distributed components	No	No

ADS	Time domain	Frequency domain
Lumped components	Yes	Yes
Distributed components	Yes	Yes