Quick Start for
Advanced Design System (ADS) in
Power Electronics Applications

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Evaluate ADS for design of power electronics

New devices (SiC, GaN) and their fast edges require new thinking about EDA tools

- Need Harmonic Balance: Yields steady state solution rapidly
- Three reasons to apply an EM field solver to your "virtual prototype":
    1. PCB traces and vias add significant parasitic impedances to your circuit
    2. Create EM-based models of integrated magnetics
    3. Model EMI/EMC

Traditional SPICE falls short…

SPICE	Time domain	Frequency domain
Lumped components	Yes	No
Distributed components	No	No

…but ADS can tackle the issues:

ADS	Time domain	Frequency domain
Lumped components	Yes	Yes
Distributed components	Yes	Yes

How to Evaluate ADS

Overview: Three steps

1. Download and install the binaries

2. Request a no-charge 45-day evaluation license

3. Follow the click-by-click demonstration in this Quick Start guide

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Step One
Download and install the binaries

– http://www.keysight.com/find/eesof-ads-latest-downloads

Step Two
Request a no-charge 45-day evaluation license

– http://www.keysight.com/find/eesof-ads-evaluation

Step Three
Follow this hands-on demonstration

– Go to:
http://edadocs.software.keysight.com/display/eesofkcads/Workshop+on+Including+Parasitic+Inductance+Effects+on+DC-DC+Converters
..and download the archived ADS workspace (as shown below) to the "home folder" that you picked during ADS installation:

Note: If you didn't receive a Knowledge Center login with the demo license, please register now

Start Advanced Design System

– Start ➔ Advanced Design System

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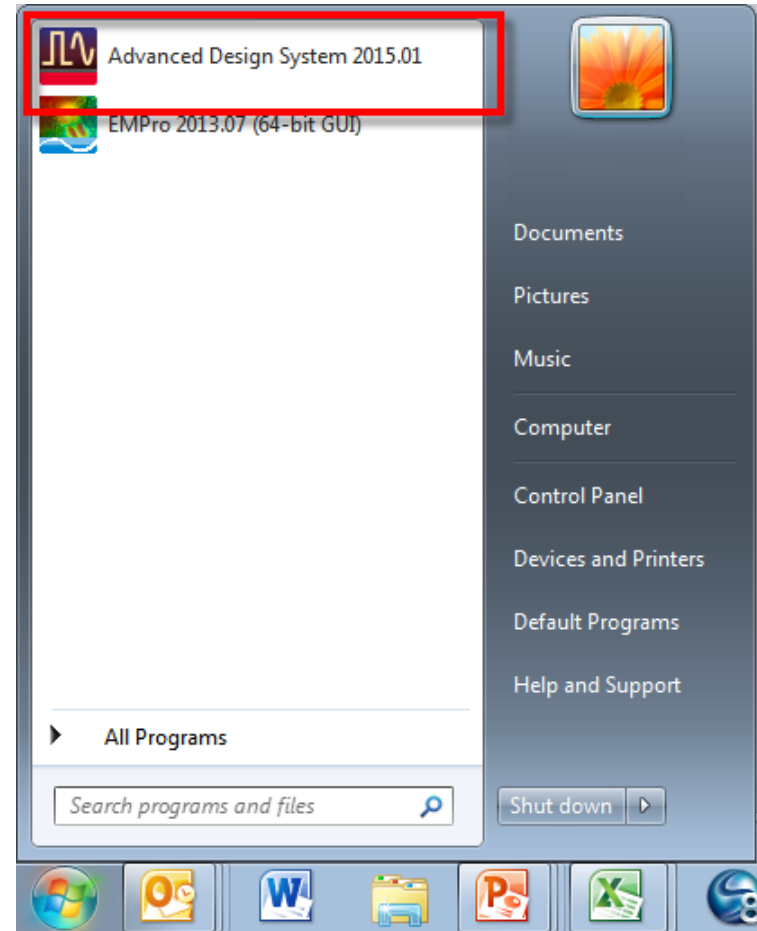
Two windows open…

– …examine but then close the "Getting Started with ADS" popup window
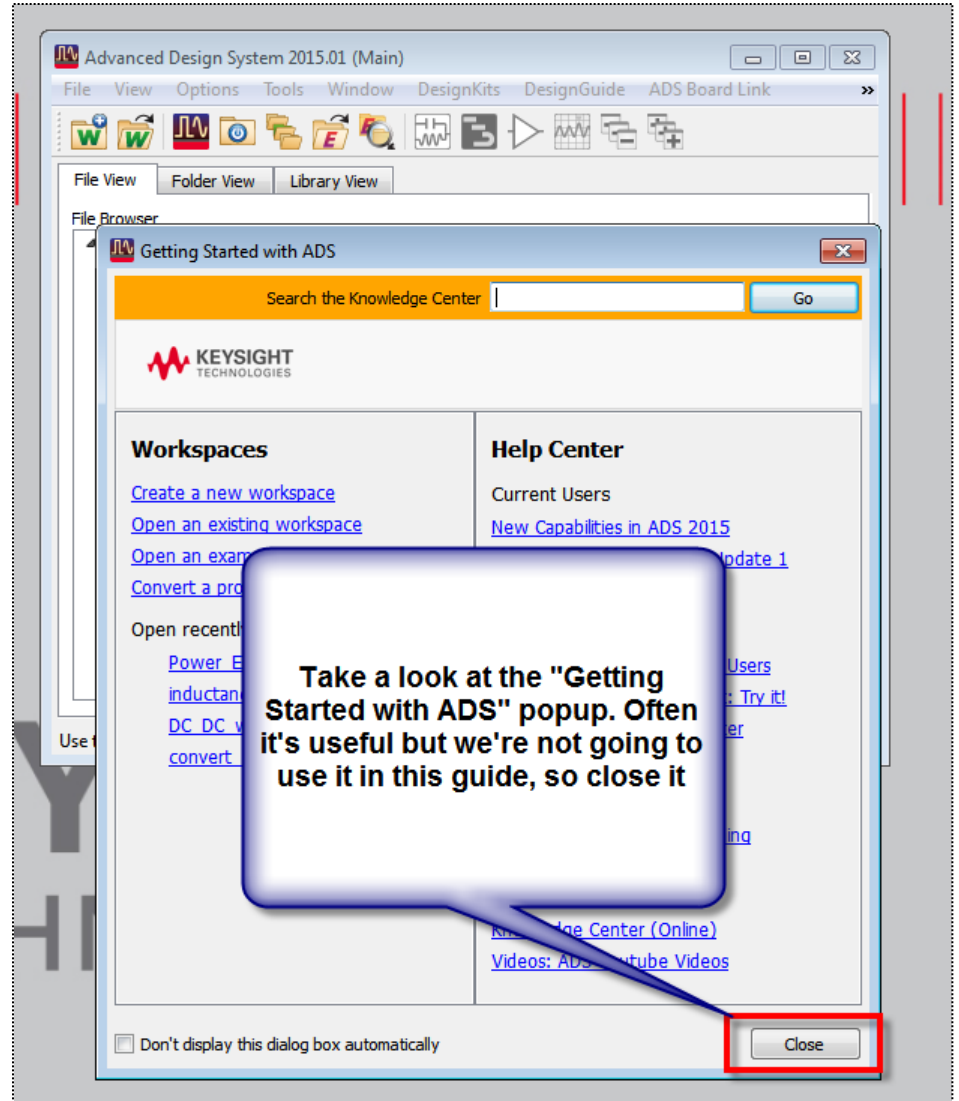
The ADS "Main" window remains…

From the Main window menu bar, select the
File ➜ *Unarchive…* dialog box

Select and open the *.7zads archive you downloaded
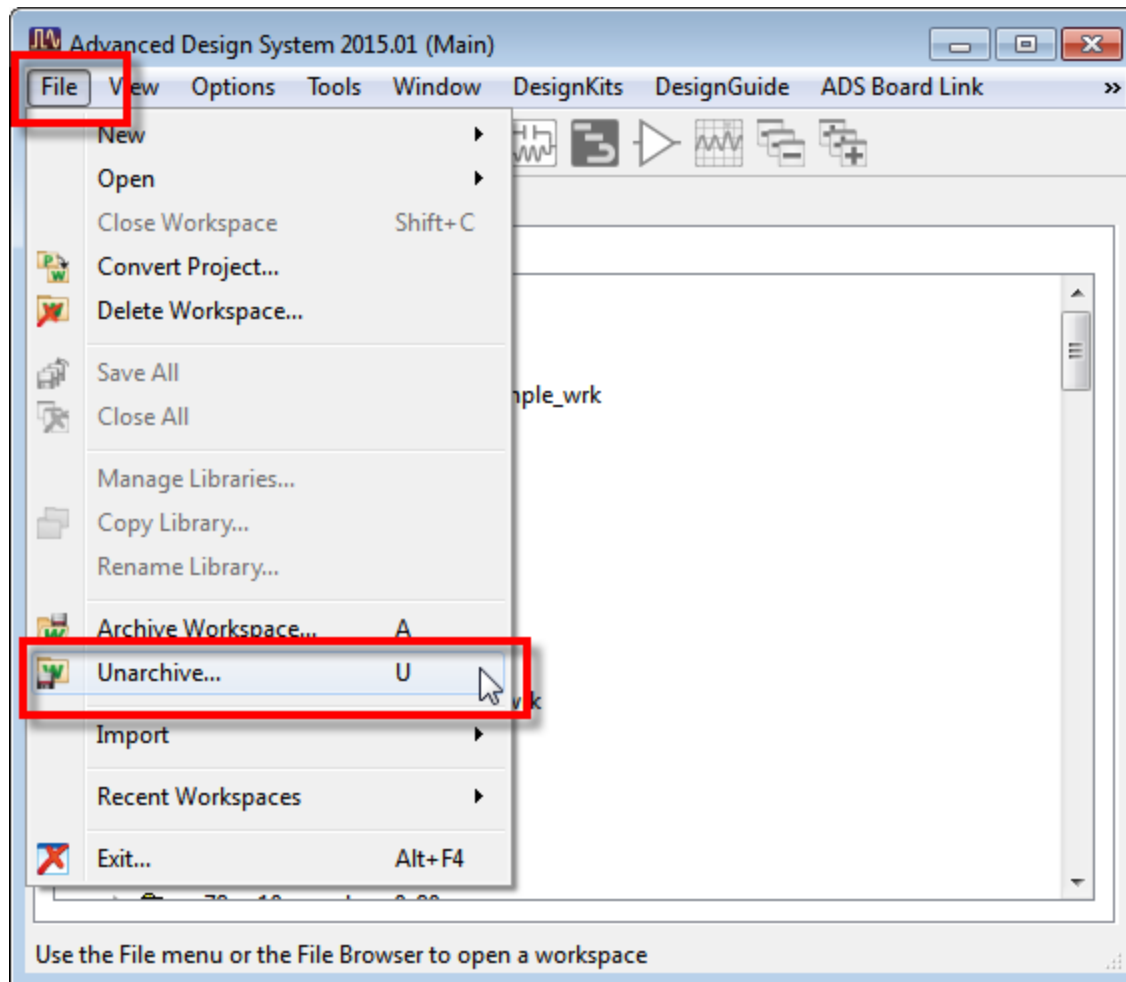
I downloaded the archive to C:\Users\cwarwick. Of course, you'll need to navigate to the folder you picked.
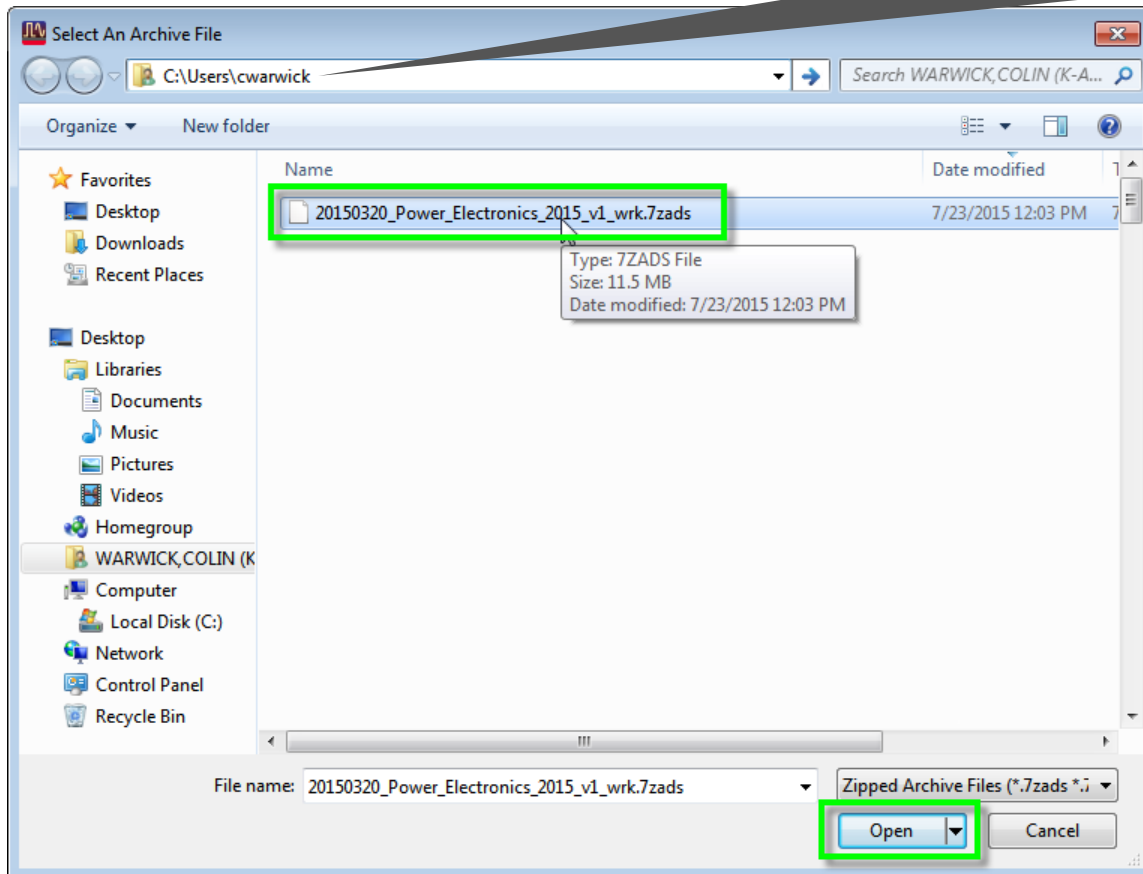
This guide doesn't cover the principles of operation but our YouTube video "How to Design DC-DC Convertors" has a refresher if you need one.

How to Design DC-to-DC Converters

Andy Howard
Applications Engineer
Keysight EEsof EDA

Keysight EEsof EDA
"How to" Video

DOWNLOAD
YOUR NEXT
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Accept the default settings of the Unarchive Wizard

– Ignore the "Next" button and just click the "Finish" button to accept all the default settings
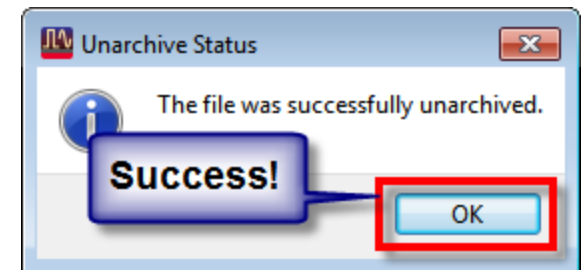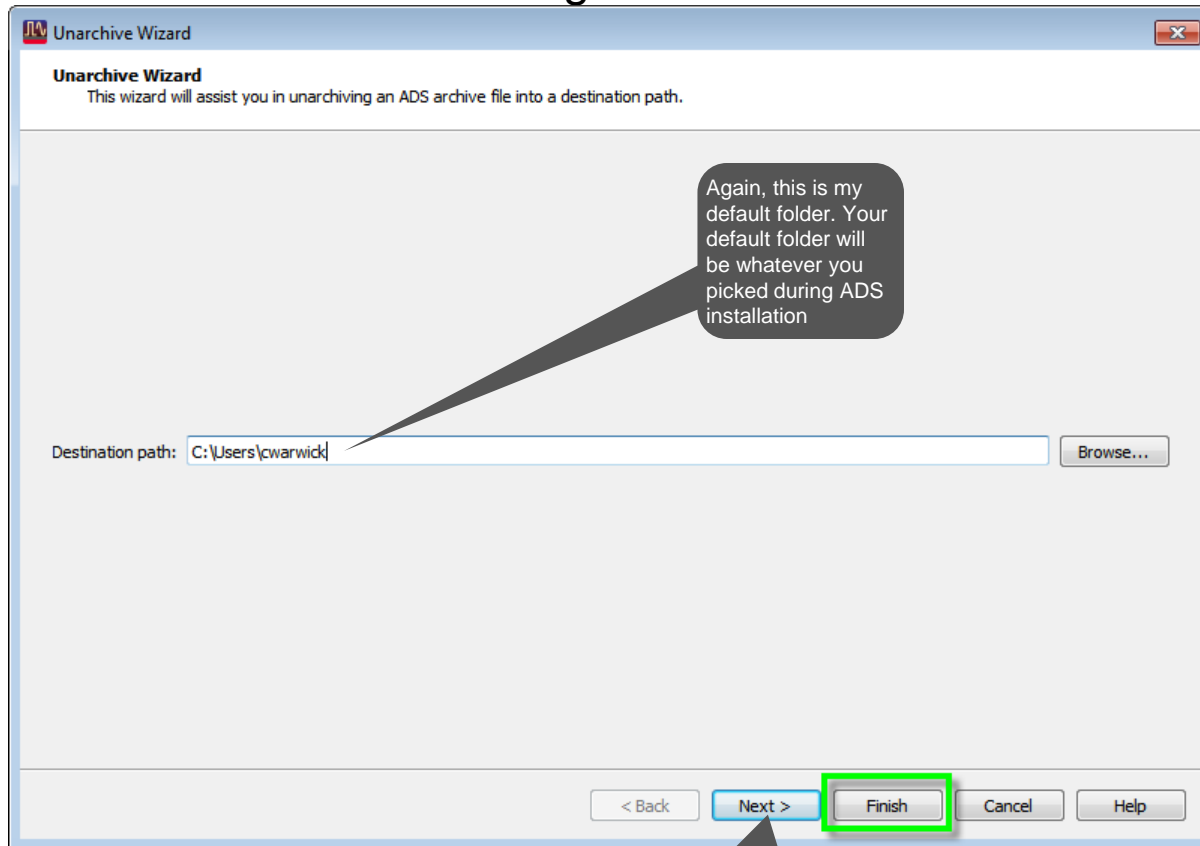
Close the Readme window, leaving "Main" open

We are going to model a switch-mode DC-DC convertor. Here's a simplified version…

We are going to model the IC behaviorally as a simple single-pole, double-throw, break-before-make switch

PV$_{IN}$

Cin

IC

L

Cout

GND

Rload

Layout
emModel
I__0

Power input

SW1

SW2

L

Cin

Cout

Output to Rload

Rload
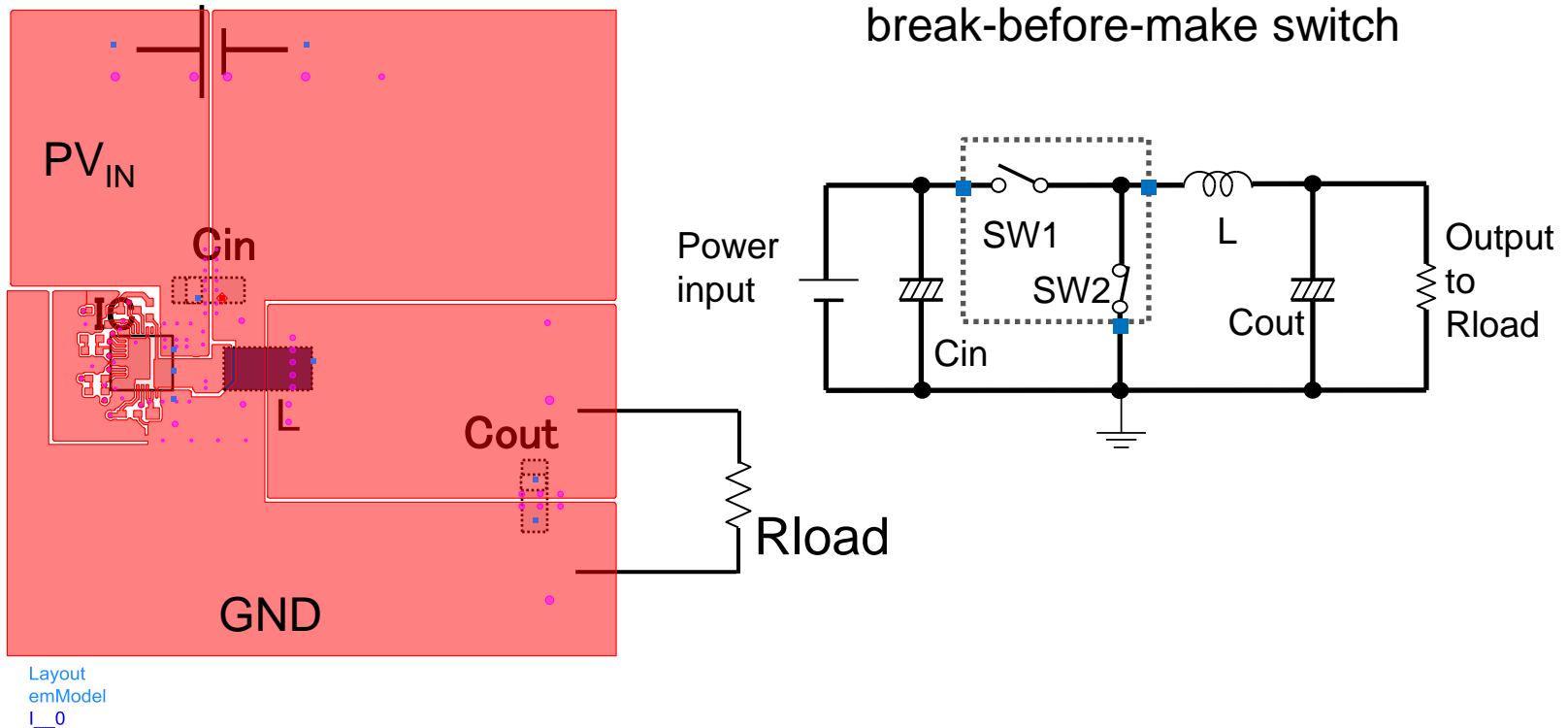
Side note: The actual IC is LTC3609 from Linear Technology, but we don't need the full vendor model for the purposes of this guide

Behavioral model of IC

PVin

SW

Output

Input power supply

SW1

SW2

L

Cout

Output to Rload

Cin

PGND

PVin

Cin

IC

L

Cout

Output

Rload

PGND

SW

Layout emModel
I__0

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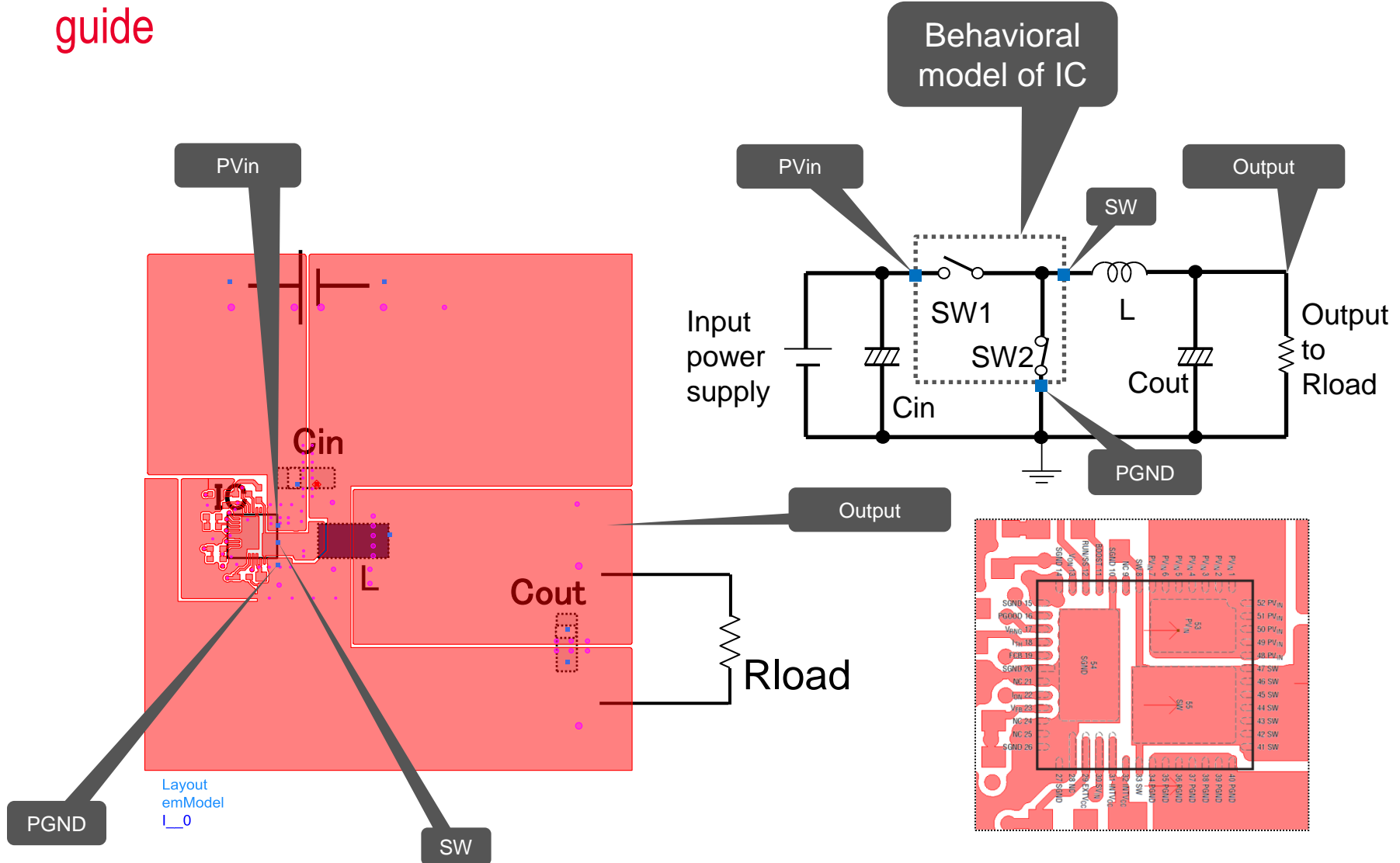
Let's see the real thing:
Open the Exercise 3 folder
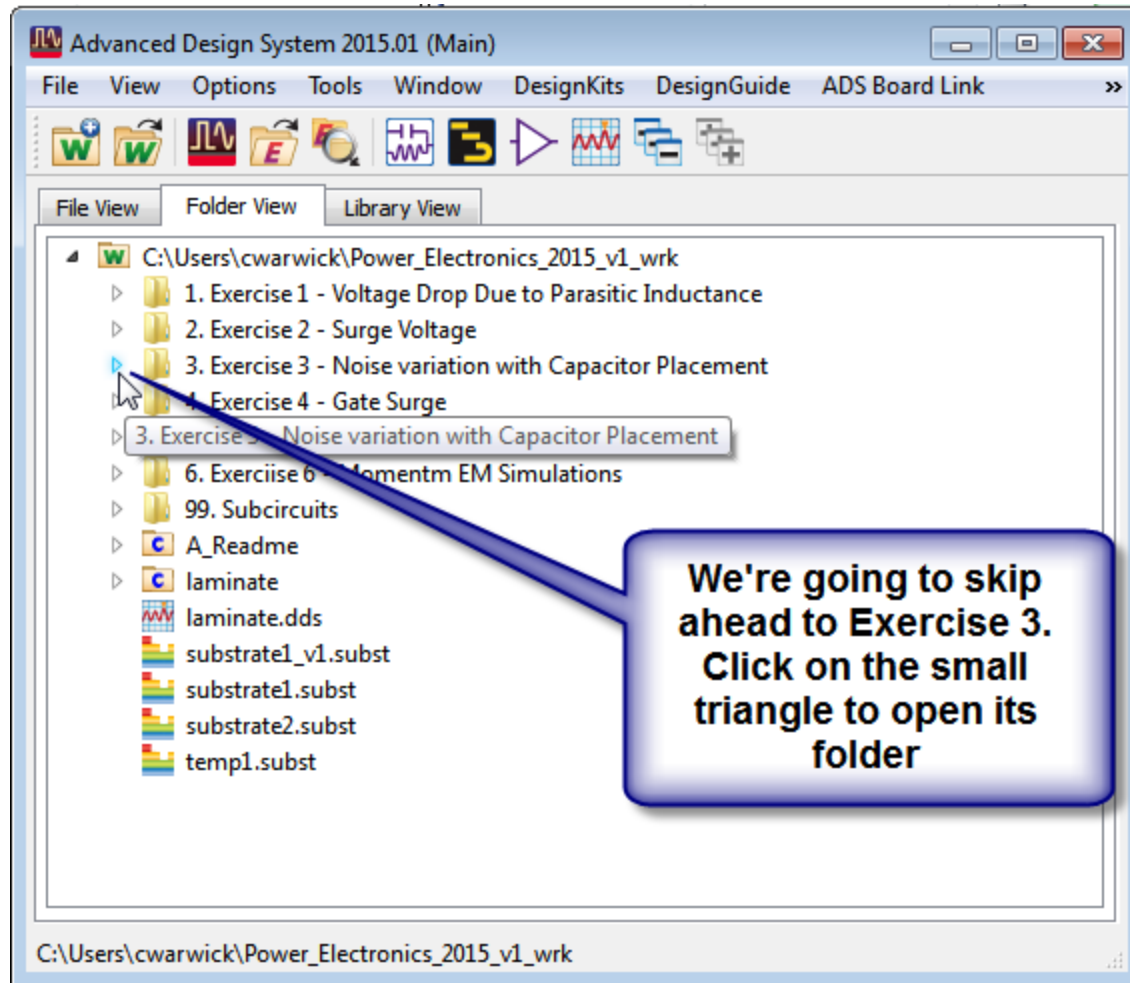
Open the cell folder "Noise_wLayout

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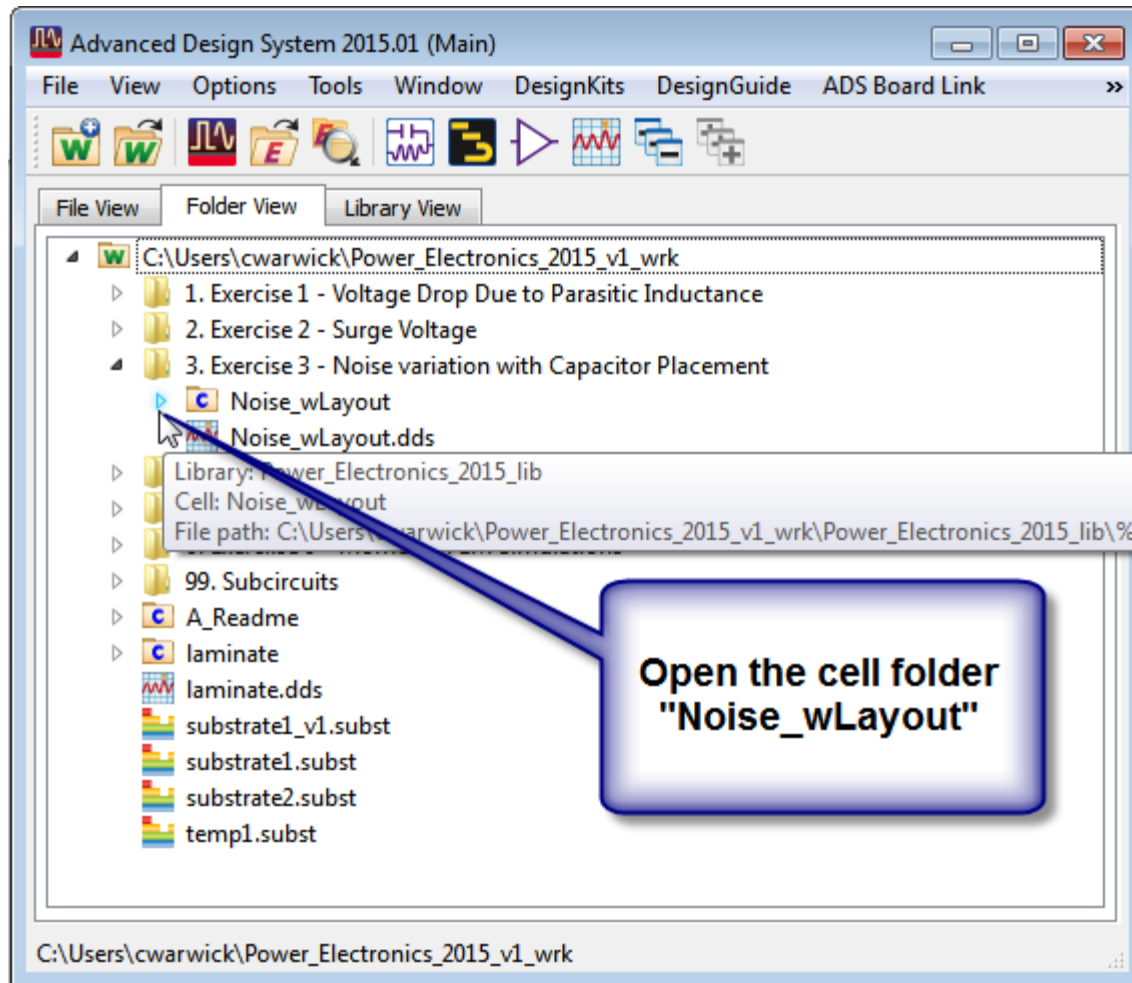
Side note: Multi-technology in ADS
Skip this slide if you like and come back to the idea later

– A **Workspace** contains one or more **Technology Libraries**

> Q. Why would you want multiple technologies? A. For example, chip, package, and board can have their own Technology Library, each with their own namespace, stack up, component library, PDK, etc.

– A **Technology Library** contains one or more design units (subcircuits), called "**Cells**"

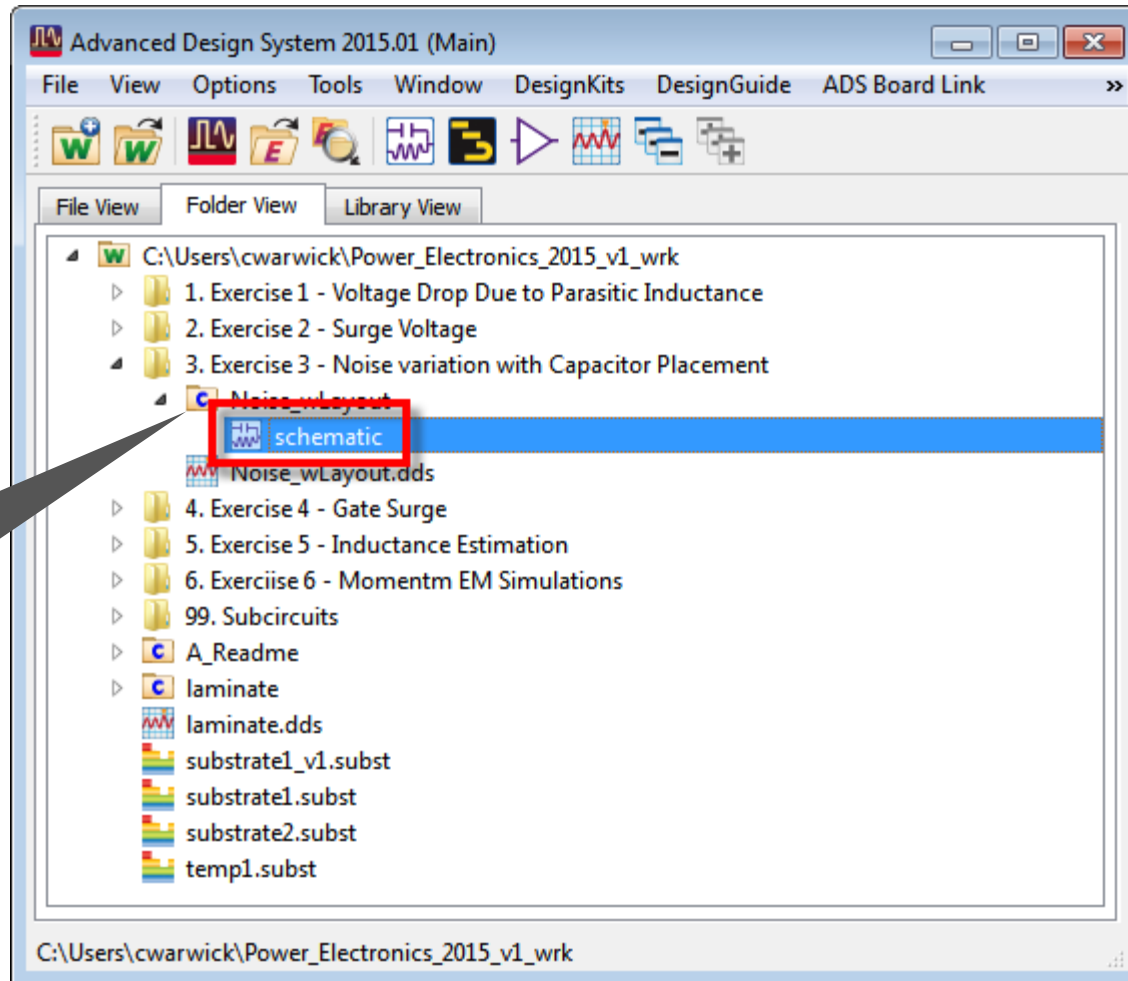> Q. Why would you want more than one? A. You might want hierarchy e.g. subcircuit cells instantiated on a top-level circuit cell. You can even instantiate a cell from one tech. library inside of a cell from another. For example, to place a chip in a package, and a package onto a PCB, just like the real world.

– A **Cell** can be viewed in one or more ways, called "**Views**"

> Q. What are the names of some Views? A. The "black box" view is called "Symbol view", the circuit view is "Schematic", the flat physical view is "Layout view", the perspective physical view is called "3D layout view" and so on

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Double click on "schematic" view of the Noise_wLayout cell

Folders that contain Cells and Views of the Cell have a letter "C" on them

There is a lot going on here, so maximize the window, and let's take a quick tour…

The top-level schematic has a simulation controller

Note: Transient is just one of many circuit simulators available for ADS…

– In this particular case we are using the time-domain SPICE-like simulator in ADS called "Transient"

– It includes a Convolution engine so it is sometimes called "Transient Convolution" or just "TC"
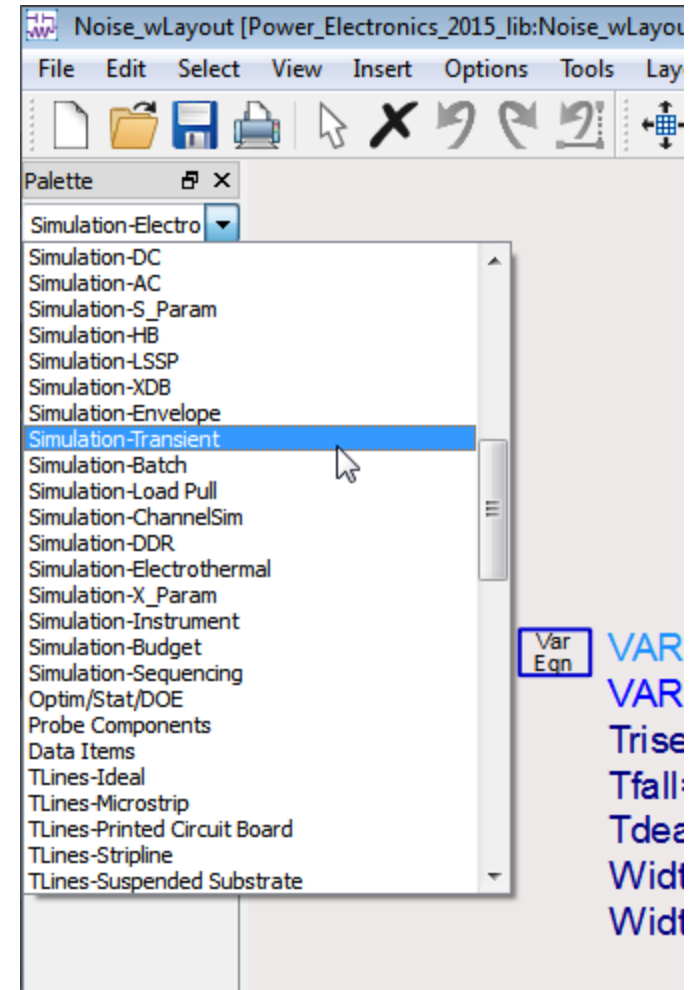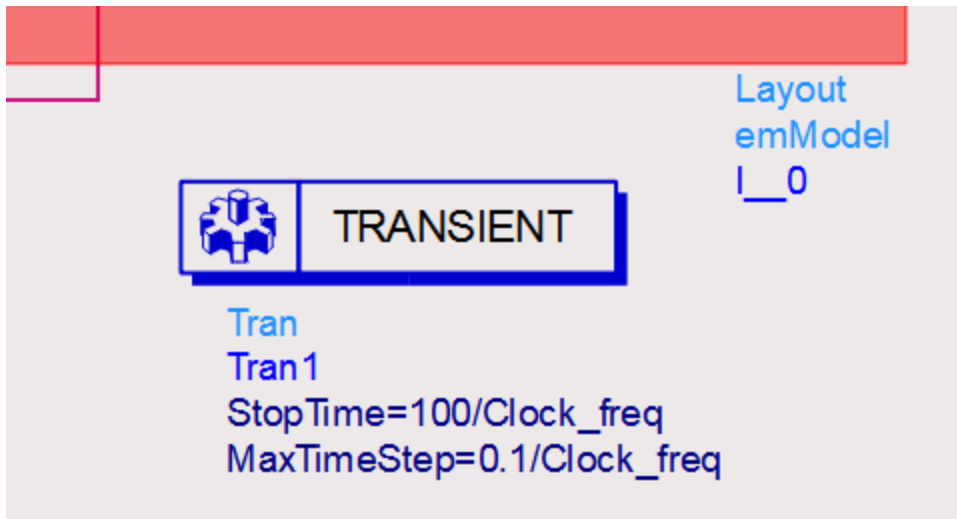
Components can be modelled behaviorally…
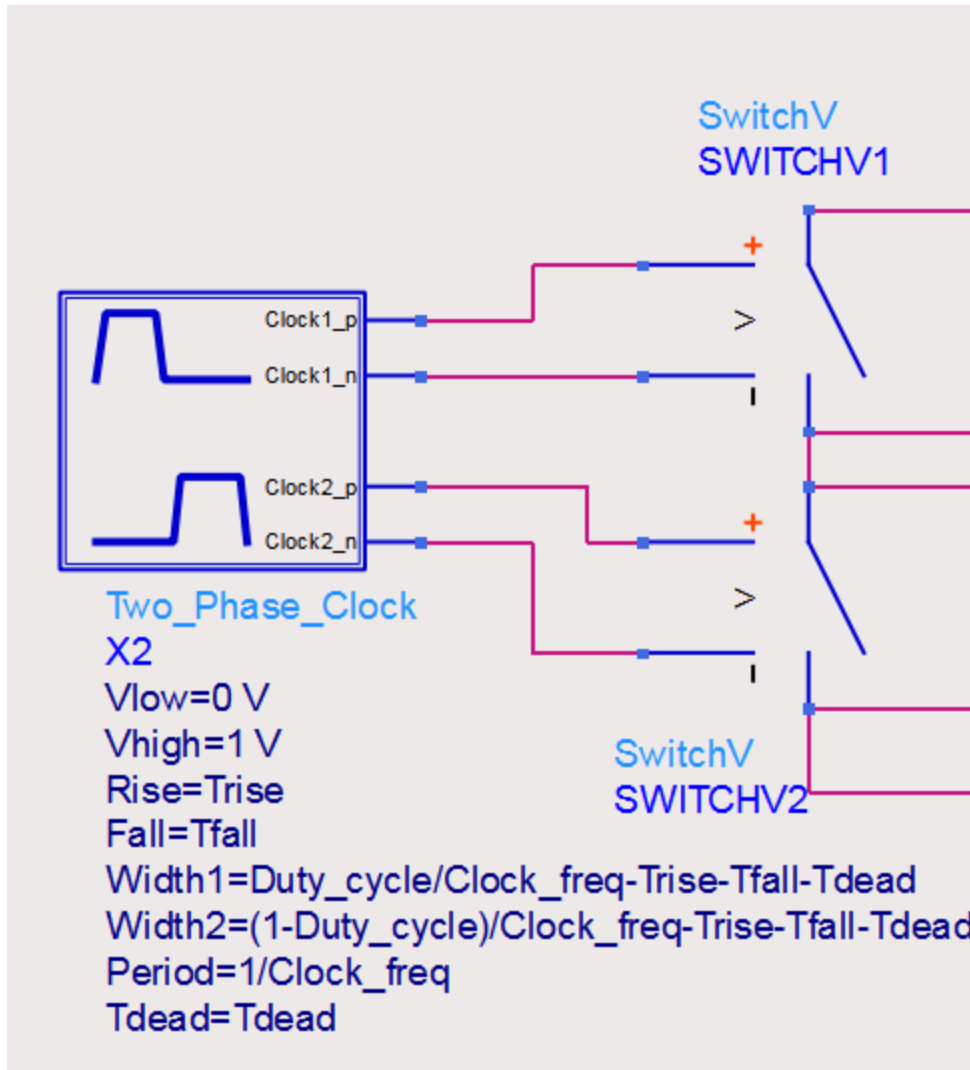
In this guide we model the IC as an ideal single-pole, double throw, break-before-make switch

SwitchV
SWITCHV1

SwitchV
SWITCHV2

Clock1_p
Clock1_n
Clock2_p
Clock2_n

Two_Phase_Clock
X2
Vlow=0 V
Vhigh=1 V
Rise=Trise
Fall=Tfall
Width1=Duty_cycle/Clock_freq-Trise-Tfall-Tdead
Width2=(1-Duty_cycle)/Clock_freq-Trise-Tfall-Tdead
Period=1/Clock_freq
Tdead=Tdead

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…or using physics-based, vendor-specific "model cards"
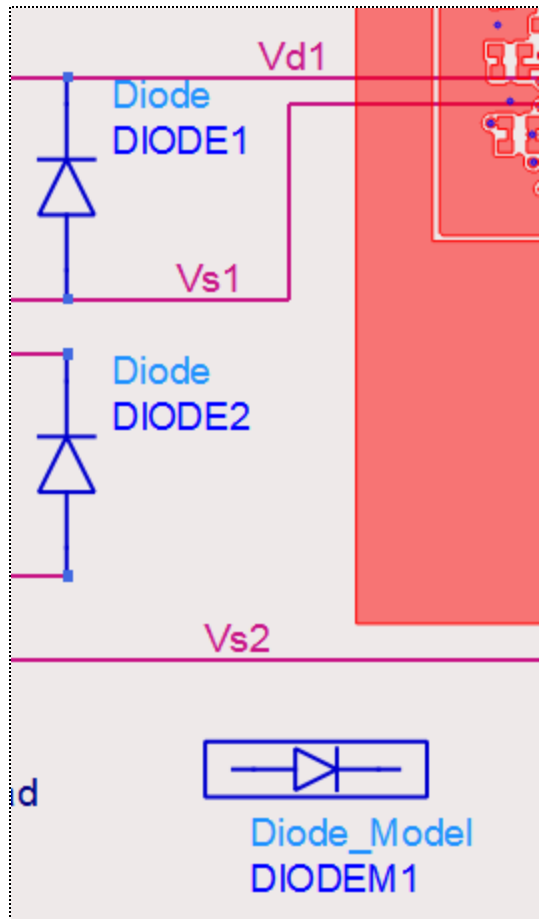
Note: Not used in this guide, but many microelectronic vendors offer models for ADS. For example, Cree:

http://www.cree.com/RF/Tools-and-Support/Model-form
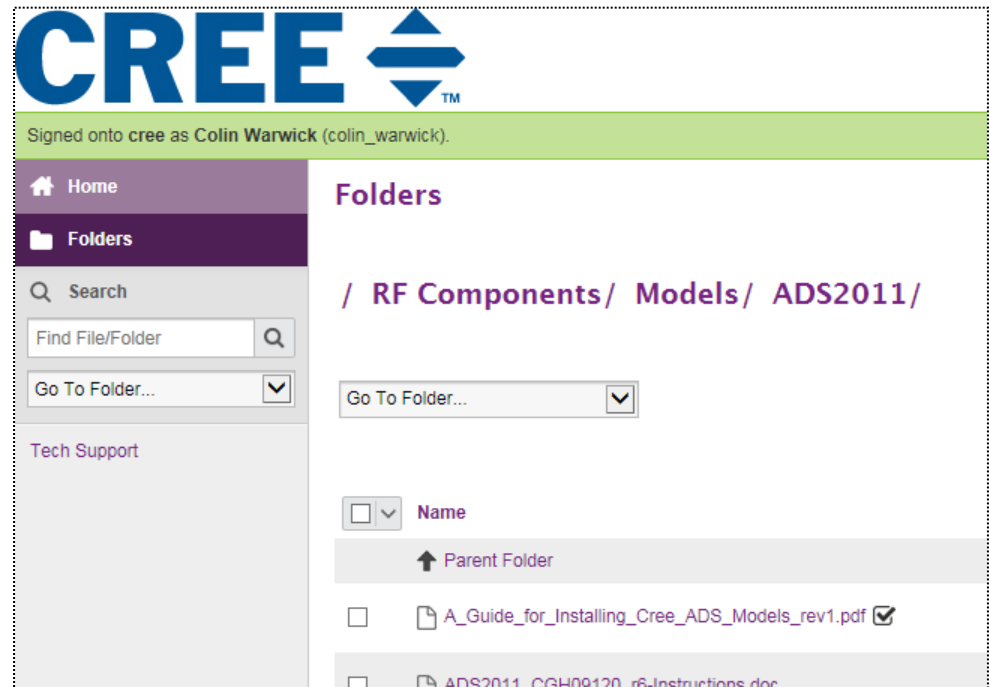
VAR blocks contain expressions evaluated *before* the simulation runs

– Can be convenient for parameterization, especially for parameter sweeps

Var Eqn	VAR
	VAR2
	Trise=100 nsec
	Tfall=Trise
	Tdead=50 nsec
	Width1=Duty_cycle/Clock_freq-Trise-Tfall-Tdead
	Width2=(1-Duty_cycle)/Clock_freq-Trise-Tfall-Tdead

| Var Eqn	VAR
	VAR3
	Clock_freq=500 kHz
	Duty_cycle=0.30

Note: ADS also has EQN or Measurement Equation blocks, which are similar to VAR blocks, but contain expressions that are evaluated *after* the simulation has run. Useful for analysis of simulation results, waveforms etc.

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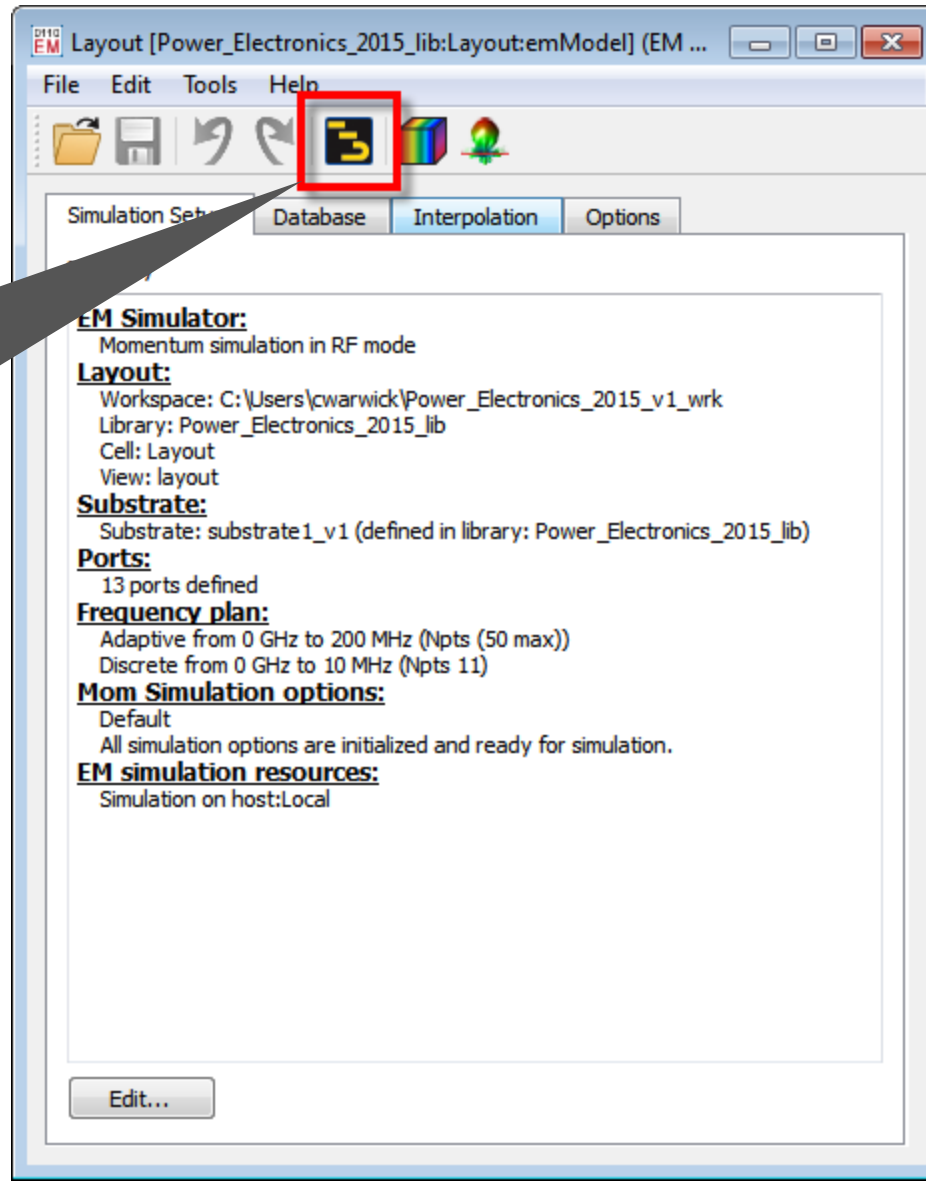
Most important: the "Look-alike" component

The EM field solver in ADS can extract a model of the layout parasitics! Right click on it and select "Push into Hierarchy" from its popup context menu

Note: The connection between the lumped component and the distributed component is represented by a magenta line with a blue square at each end
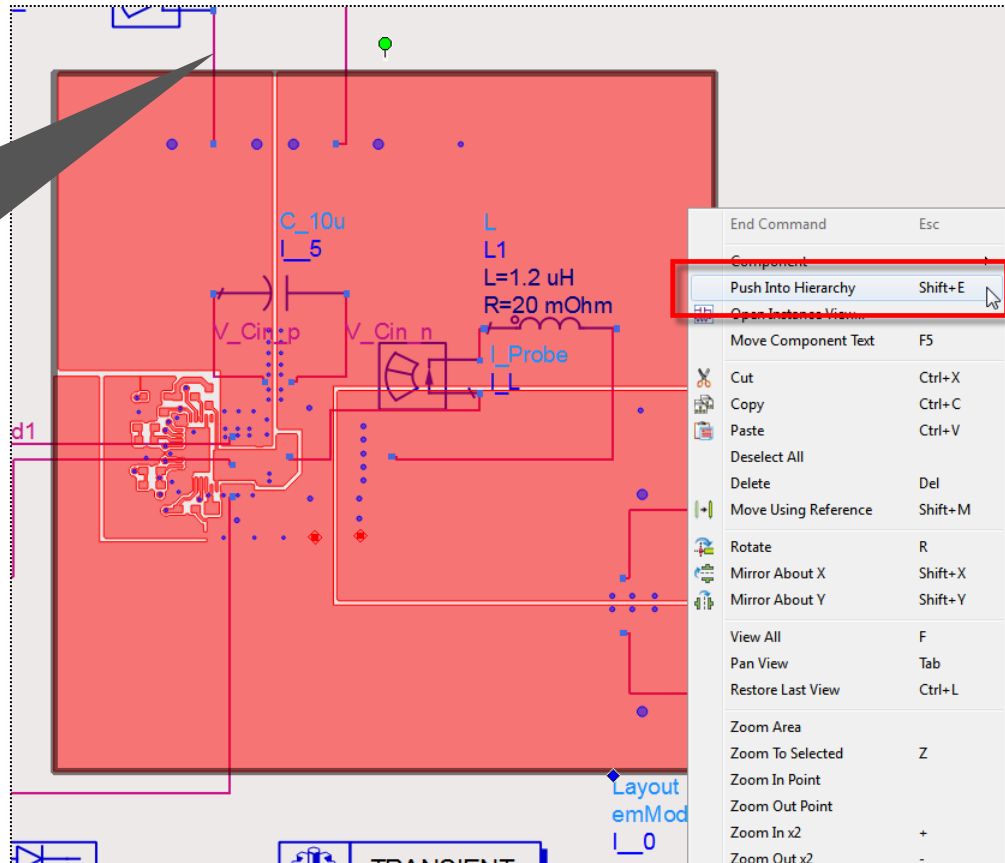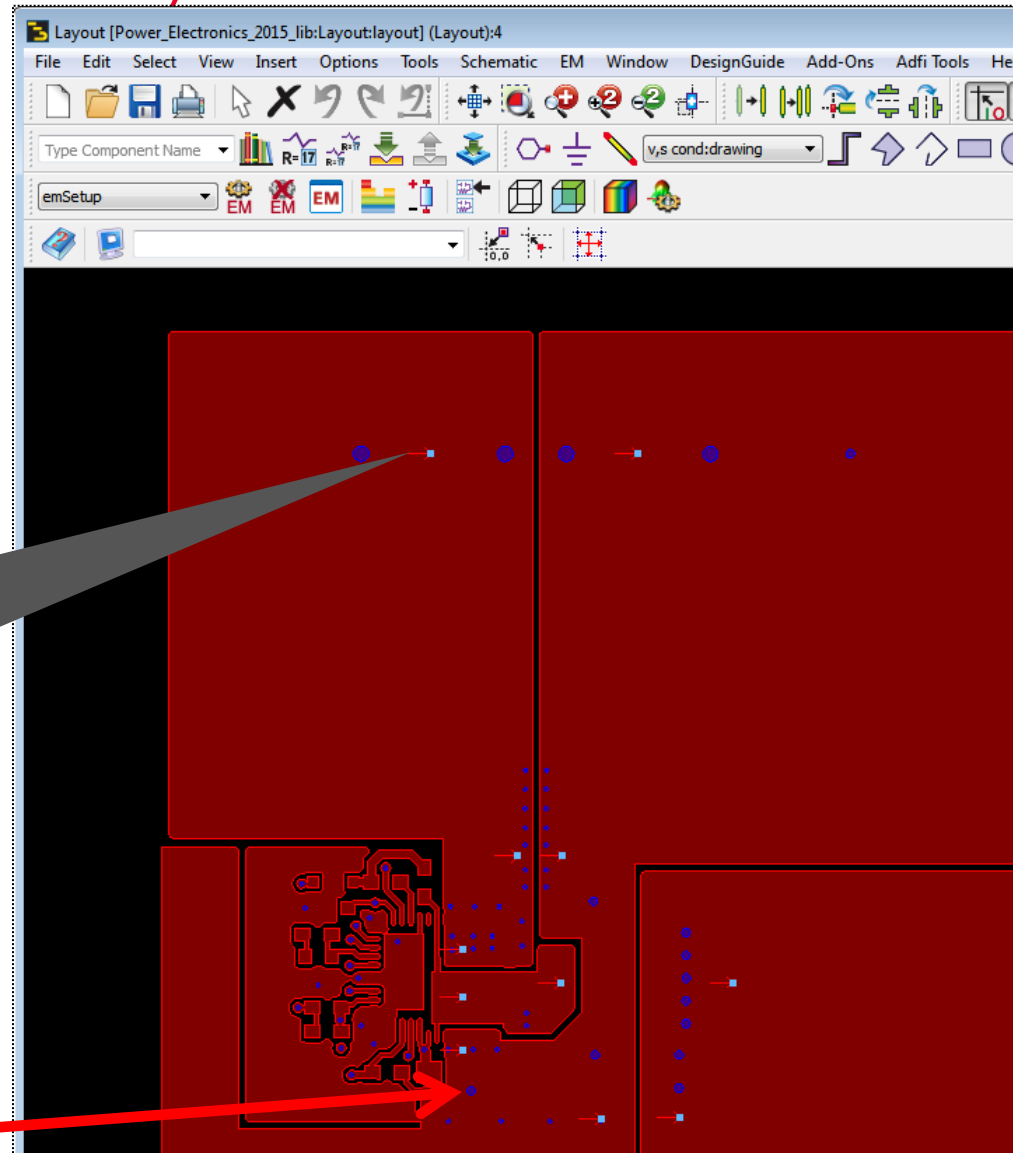
Under the hood are details of the EM model. Click on the layout icon to open the artwork

Opens the layout view of the cell called "Layout"

Layout [Power_Electronics_2015_lib:Layout:emModel] (EM ...

File   Edit   Tools   Help

Simulation Setup   Database   Interpolation   Options

EM Simulator:
Momentum simulation in RF mode
Layout:
Workspace: C:\Users\cwarwick\Power_Electronics_2015_v1_wrk
Library: Power_Electronics_2015_lib
Cell: Layout
View: layout
Substrate:
Substrate: substrate1_v1 (defined in library: Power_Electronics_2015_lib)
Ports:
13 ports defined
Frequency plan:
Adaptive from 0 GHz to 200 MHz (Npts (50 max))
Discrete from 0 GHz to 10 MHz (Npts 11)
Mom Simulation options:
Default
All simulation options are initialized and ready for simulation.
EM simulation resources:
Simulation on host:Local

Edit...

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The EM model is based on 1) the actual PCB artwork…

Note: In layout view, a "pin" is represented by small cyan square with a red arrow coming out

The dark blue circles are via holes

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…and 2) the material properties of the stackup of the technology library that the layout is in

Optional: Click the EM cog icon, and click "Yes" to re-build the EM model dataset
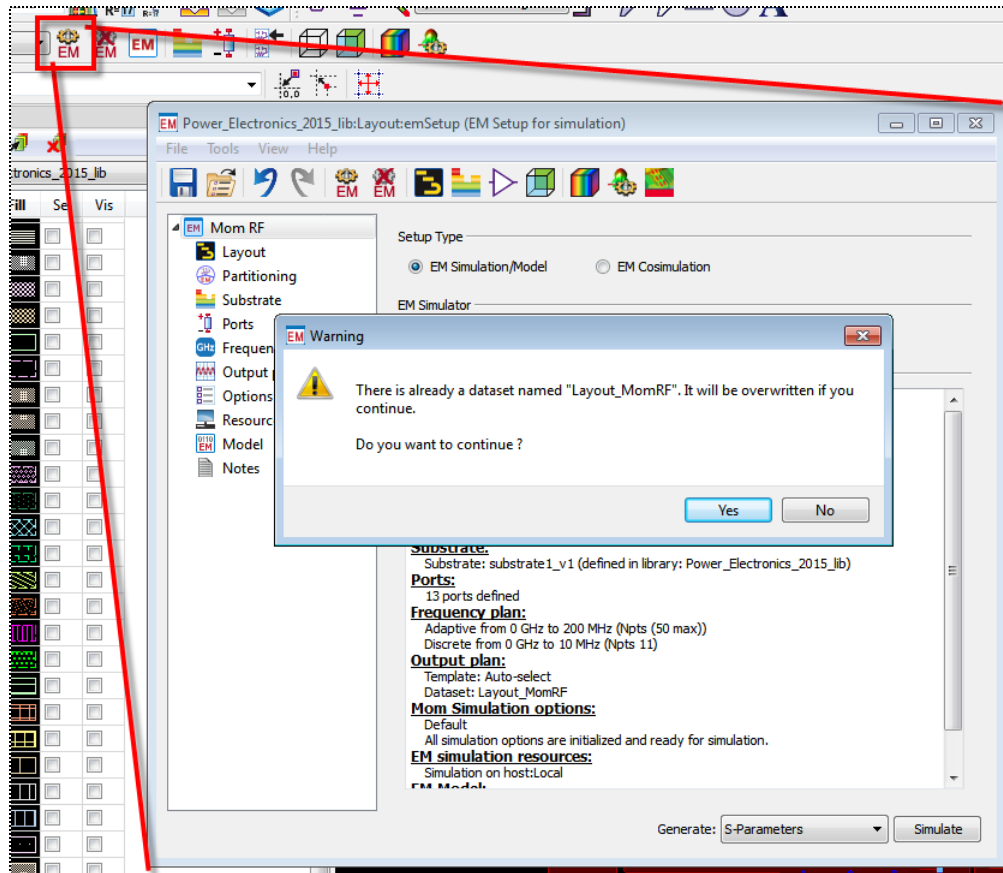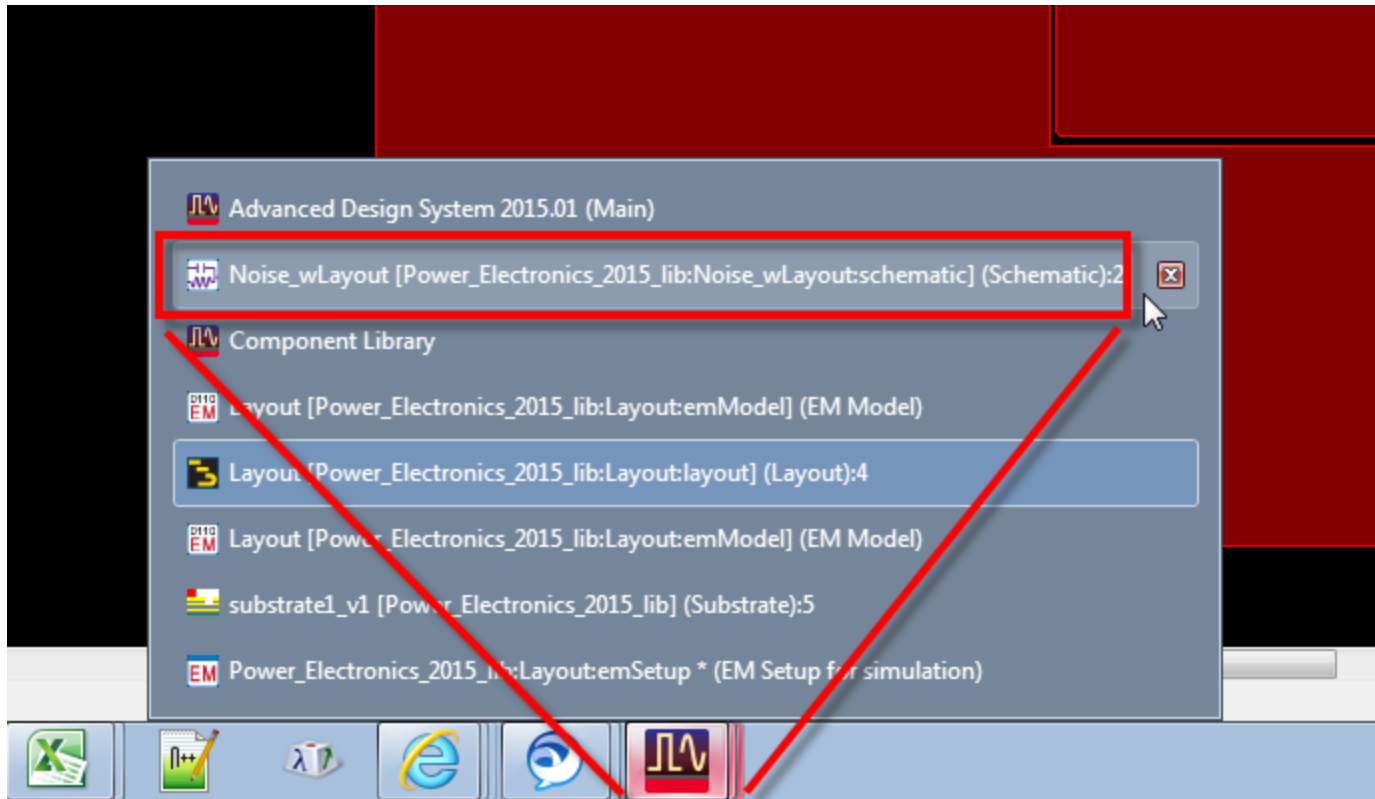

Caution: If you perform this optional step, the EM simulation takes about 20 minutes on a typical PC. This step is optional because we already ran the EM simulation for you and saved the resulting dataset in your workspace.

Side note: The EMPro add-on to ADS can build EM models of arbitrary 3D shapes like magnetics and integrate them with layout and schematic

– Advanced topic: not covered further in this guide

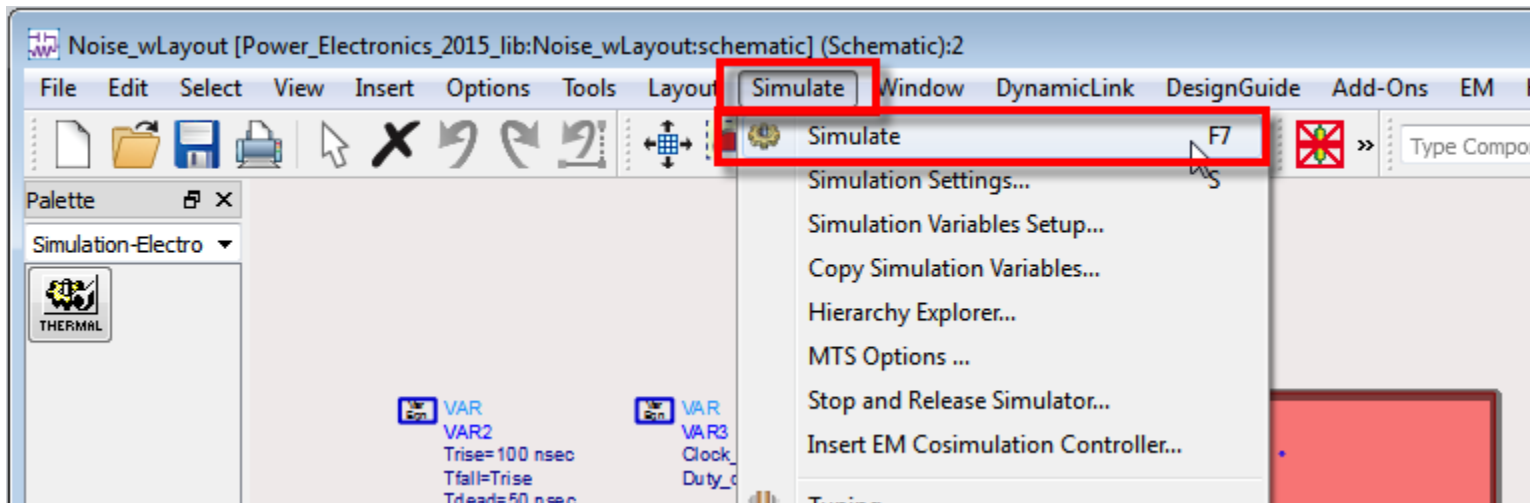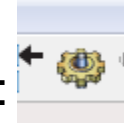– Contact your Keysight rep for more info

EMPro 3D Design

Common Database

ADS Layout (3D View)

ADS Schematic

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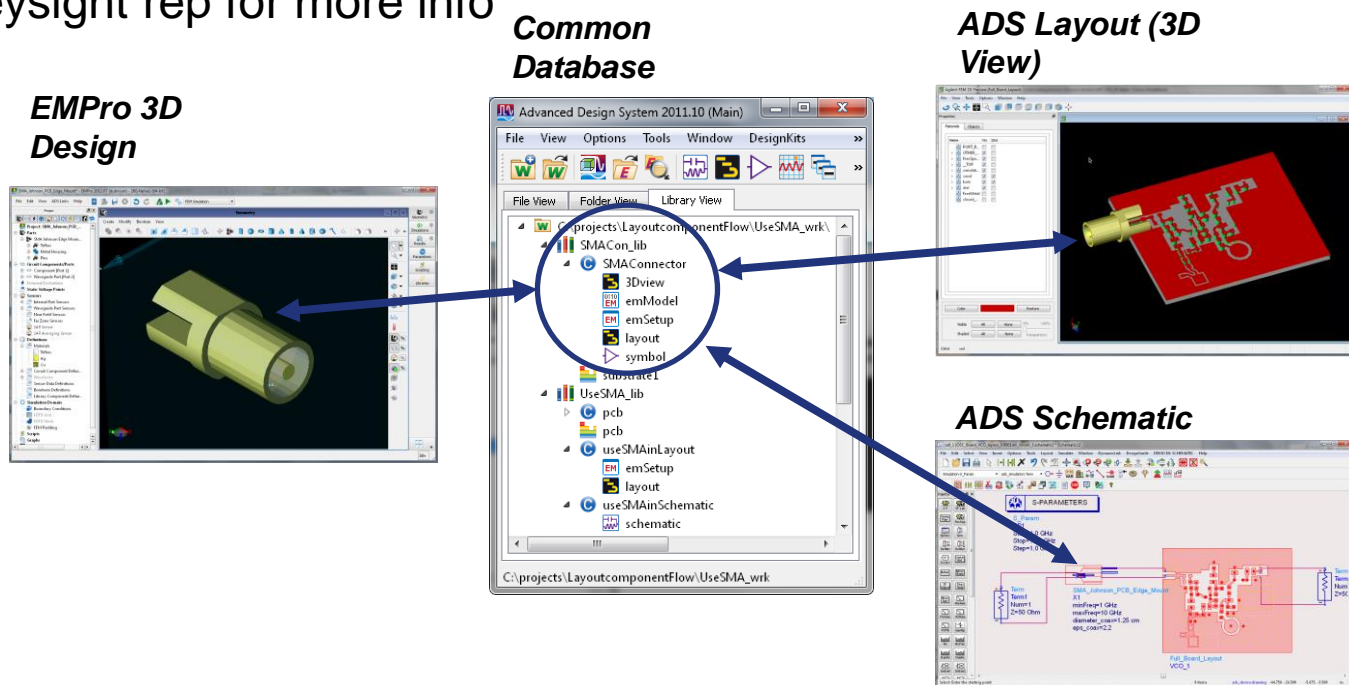
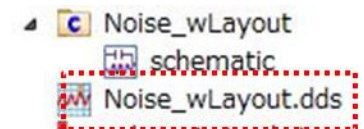# From the Windows task bar, bring the original schematic back on top

From the schematic menu bar, select Simulate ➔ Simulate

Note: You could also:
1) Use the F7 hotkey or
2) Click the simulate (cog wheel) icon in the tool bar:

After a few seconds, the simulation finishes, and the data display window opens automatically…

Side note: The *.dds file extension means "data display server"

Rescale the Y-axis in the baseline ripple plot

…in preparation for comparing this "good" design with the "bad" one that we'll do next

Next let's see the effect of layout parasitics on ripple…
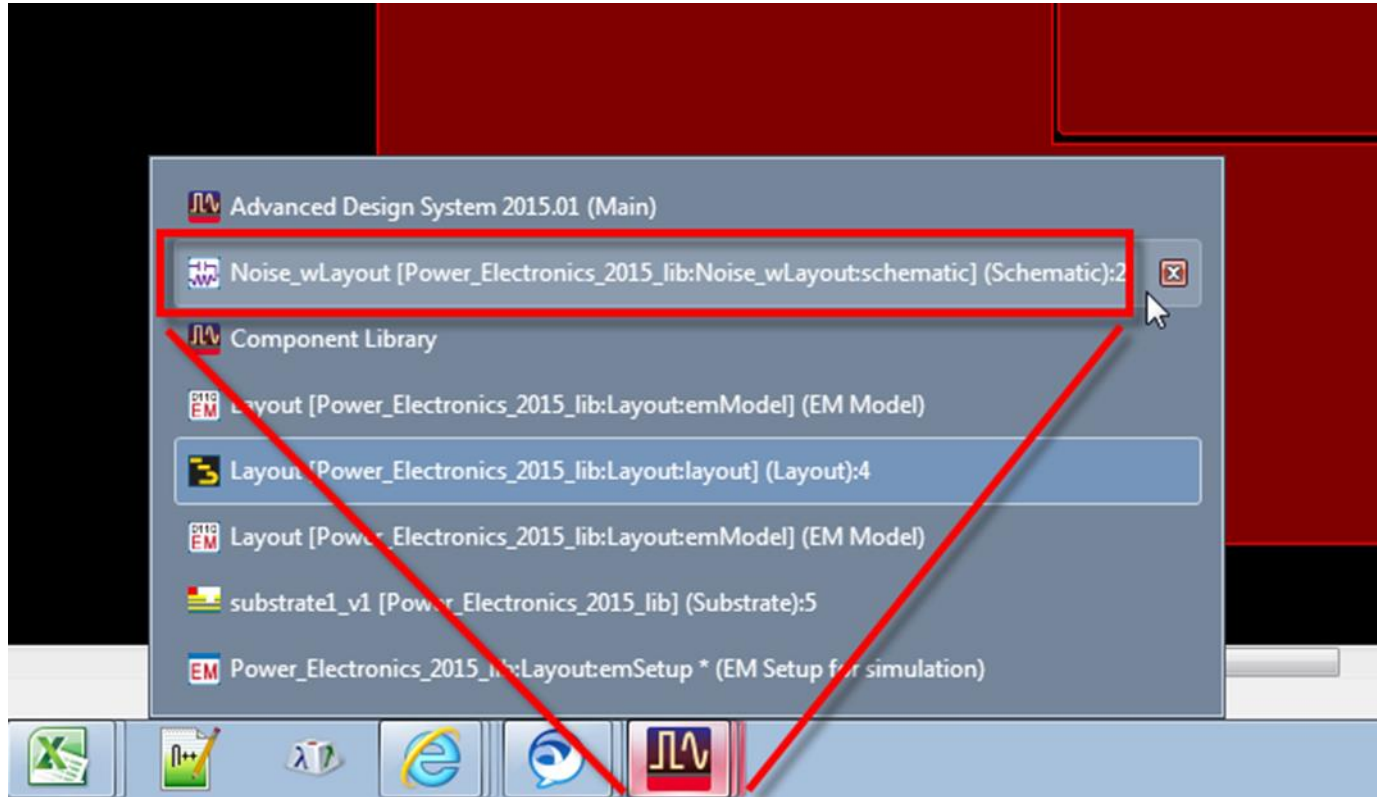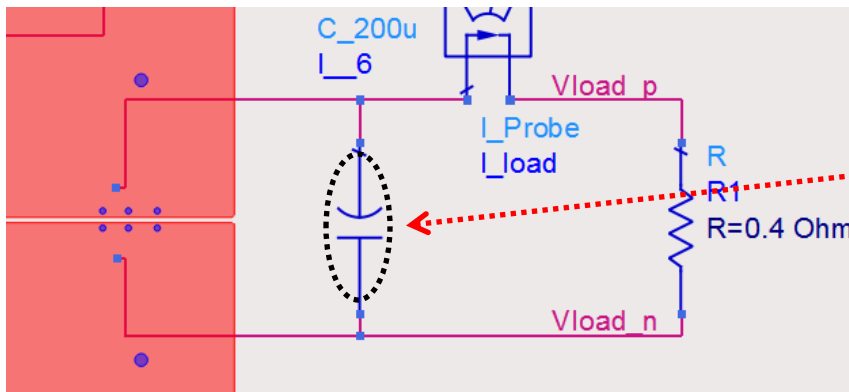
Parasitic impedance causes more ripple noise
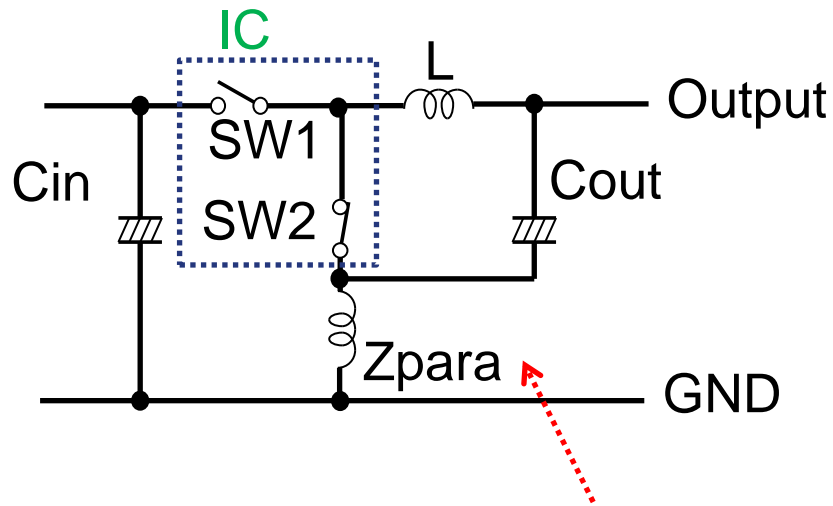
Let's show what happens to ripple if we add a parasitic impedance by artificially increasing the trace length between Cout and the output ports to Rload
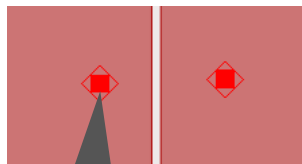
Bring the schematic window back on top

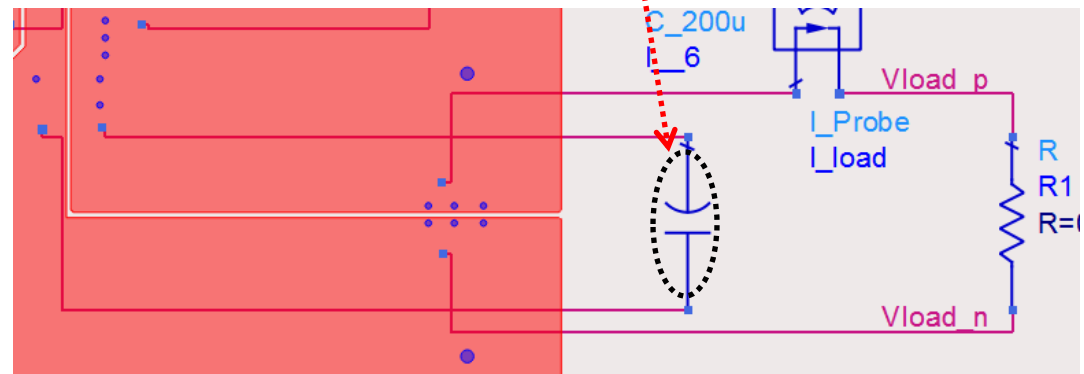# We are going to change the connection points of C_200u (Cout)

Exact steps are on the next slide…
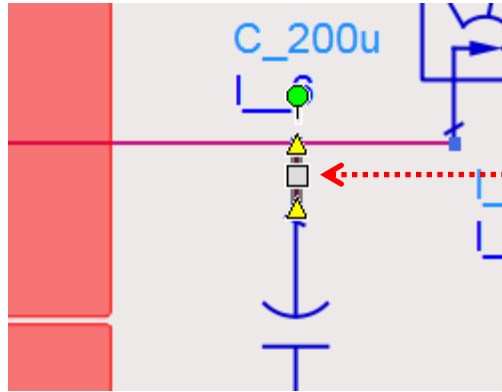

Change in placement on the PC board

Note: Before you connect them, pins are red diamonds

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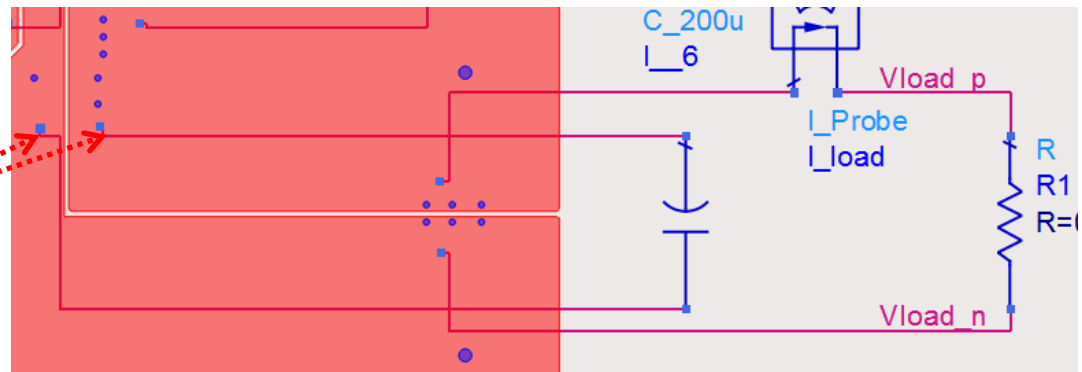TECHNOLOGIES

How to change the connection points

1. Left click to select the wire. Next, hit the Delete key. Remove the other wire connecting C_200u.

Left click here. Then press the "Delete" key. Repeat for the bottom net.

2. After clicking , left click on the nodes as shown to re-connect the capacitor.

New port connections

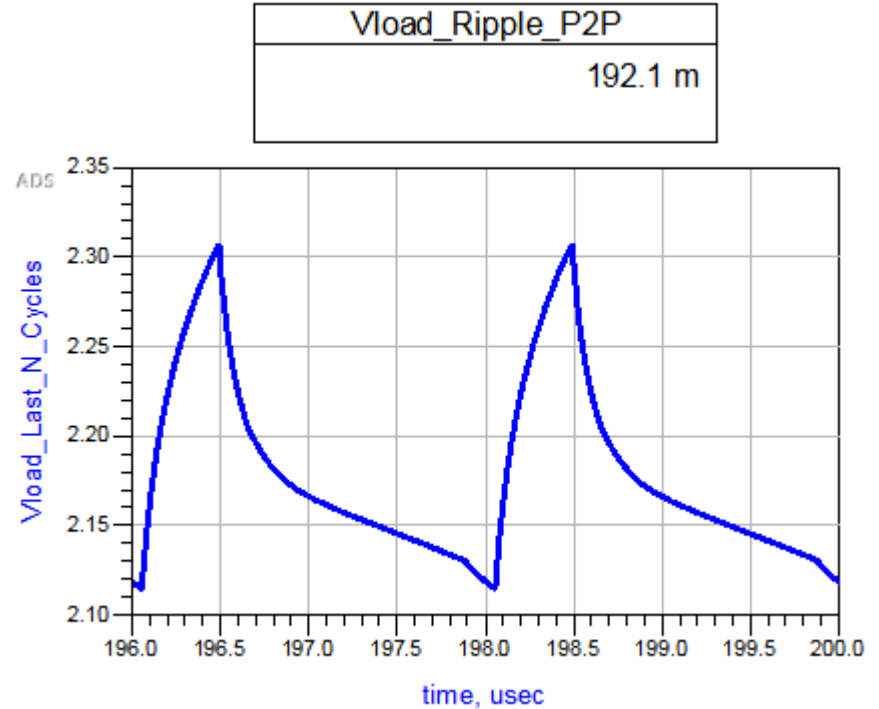# Re-run with "bad" connection points

Click ⚙ to re-run the simulation. The "display dataset" window comes into focus again.

Vload_Ripple_P2P
83.94 m

Vload_Ripple_P2P
192.1 m
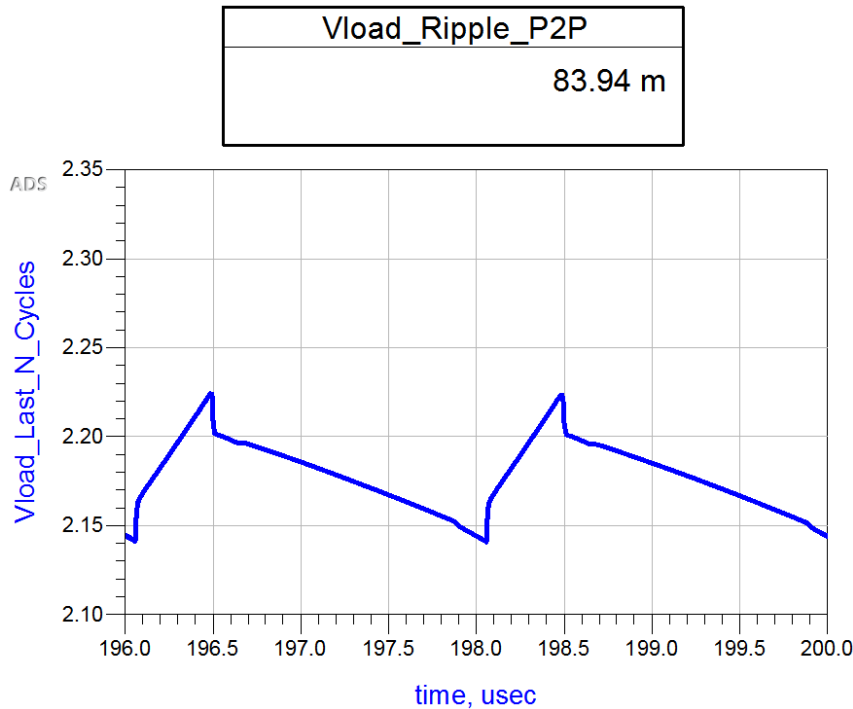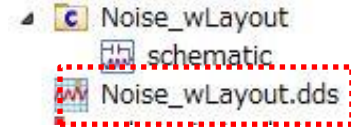
Before: Low layout parasitic   After: High layout parasitic

Note: Do Y-axis scaling on the new plot as before

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Conclusion and Next Steps

In power electronics, ADS can solve problems that SPICE alone cannot

This guide has just a small taste! Contact your Keysight EEsof EDA expert for further e-learning material to meet your needs!
http://www.keysight.com/find/eesof-support

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toll-free	1 800 829-4444 Press #, then 2	Sales Request
fax	1 800 829-4433	
hours	8:00am - 8:00pm ET, Mon - Fri	Phone Directory and Holiday Schedule
address	P.O. Box 4026 Englewood, CO 80155-4026 United States	

SPICE	Time domain	Frequency domain
Lumped components	Yes	No
Distributed components	No	No

ADS	Time domain	Frequency domain
Lumped components	Yes	Yes
Distributed components	Yes	Yes

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